
# Analog to Digital
# AD1, AD2, AD3
# Function Modules

# MODULE MANUAL

# Revision History

| Revision | Revision Date | Description | Author |
|---|---|---|---|
| A | 2/1/2018 | Initial release | SL |
| A1 | 3/5/2018 | ECO C05412, updates to module manual consistency | SL |
| A2 | 3/28/2018 | ECO C05470, update to spec and filter break frequency register based on engineering input | SL |
| A3 | 5/21/2018 | ECO C05614, update to common mode rejection | SL |
| | | | |

# Table of Contents

## Introduction

This module manual provides information about the North Atlantic Industries, Inc. (NAI) Analog-to-Digital Function Modules: AD1, AD2, AD3. These modules are compatible with all NAI Generation 5 motherboards.

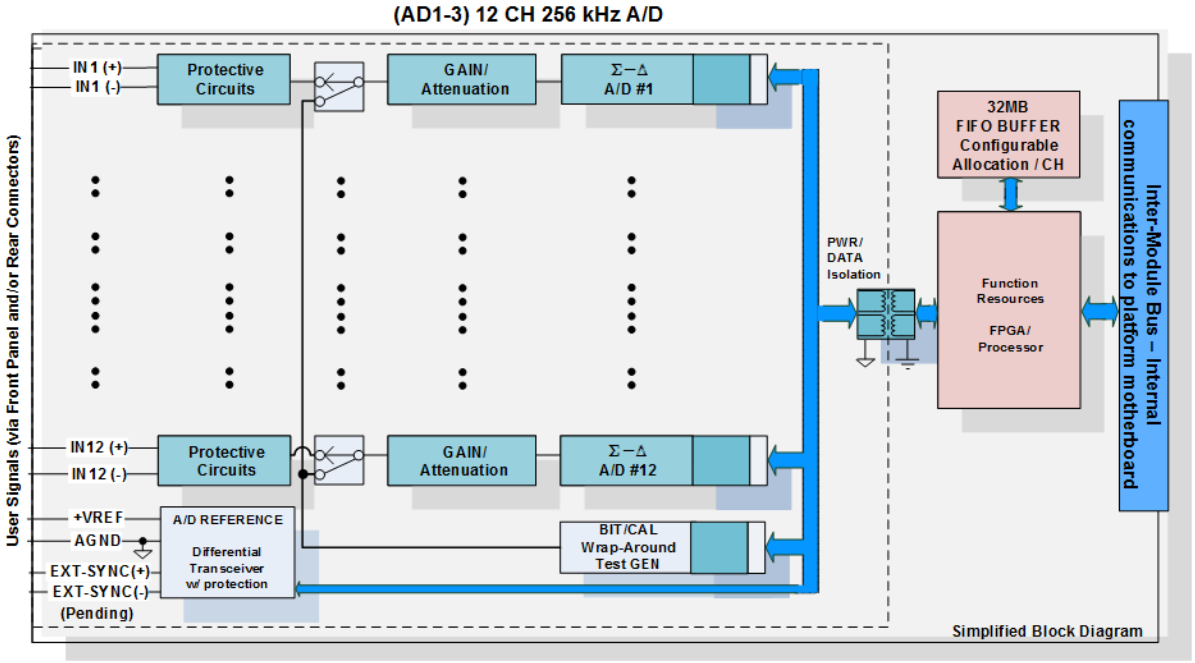
Modules AD1, AD2 and AD3 are 12-channel A/D module(s) with (up to) 24-bit Sigma-Delta A/D converters for each individual channel with maximum programmable expected full scale range inputs of 10V, 100V, and ±25 mA (current only) respectively. The A/D converters have programmable sample rates of up to 256 kHz.

## Features

- The input range is field programmable for each channel. The ability to set lower expected, full-scale voltage ranges assures the use of the full resolution.
- Each channel includes an anti-aliasing filter followed by a “brick wall” filter and a digital second-order IIR low-pass filter with a programmable breakpoint that enables users to field-adjust the filtering for each channel.
- All channels have continuous background Built-In-Test (BIT).
- The module(s) also include extended A/D FIFO buffering capabilities for greater storage/management of the incoming signal samples (data) for post processing applications.
- Programmable FIFO buffer thresholds maximize data flow control (in and out of the FIFO). Incremental relative time-stamping between samples is also provided as a programmable option.

## Specifications

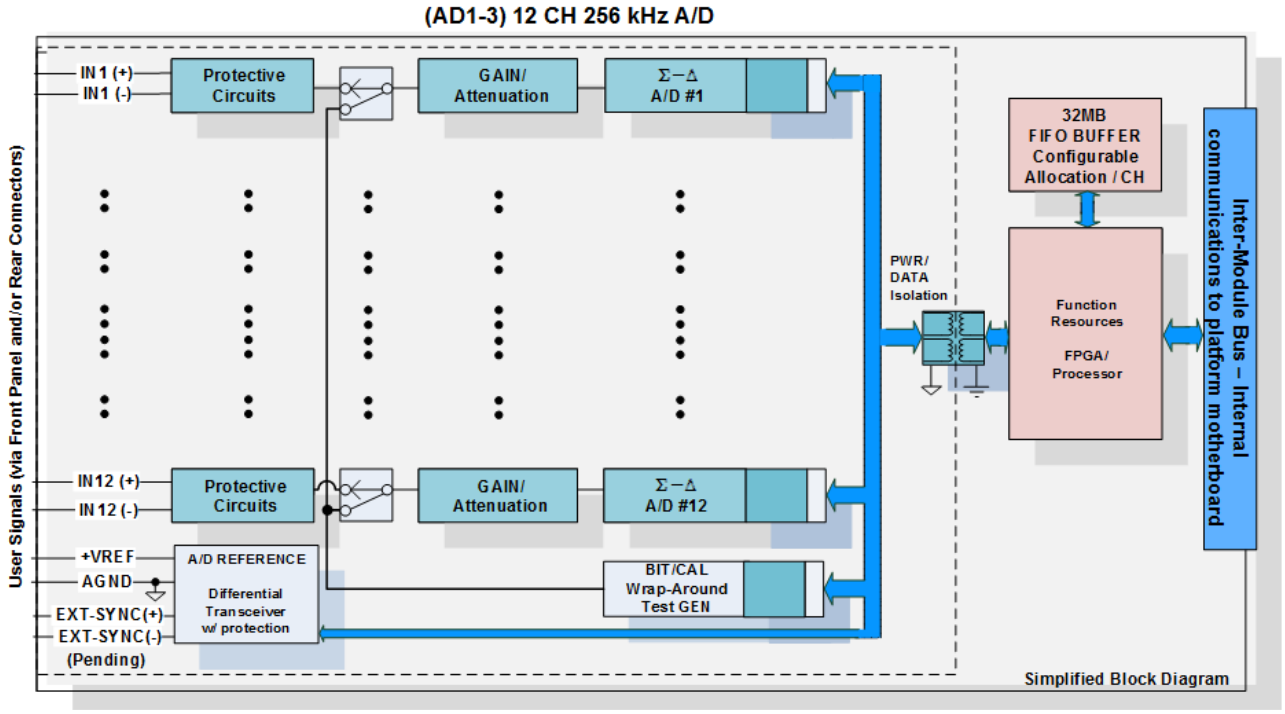
### Analog-to-Digital Module AD1 – 12 Channels (±10.0 to ±1.25 VDC)




| | |
|---|---|
| **Resolution:** | 24-bit Sigma-Delta A/D converters. One per channel. |
| **Input Format:** | Differential voltage (may be used as single-ended by grounding one input). |
| **Input Scaling:** | Twelve (12) bipolar or unipolar channels (volts).<br>Programmable, per channel, as Full Scale (FS) range inputs of 10.00, 5.00, 2.50 or 1.25 volts where range is -FS to +FS or 0 to FS VDC. The ability to set lower voltages for FS assures the utilization of the full resolution. |
| **Overvoltage Protection:** | No damage up to ±12 V continuous; ±30 V momentary |
| **Open Input Sense:** | This module will sense and report unconnected inputs. |
| **Input Impedance:** | 1 MΩ min. |
| **Linearity/Accuracy:** | ±0.05% FS range over temperature (voltage), to 16-bits |
| **Gain Error:** | ±0.05% FS range |
| **Offset Error:** | ±0.02% FS range |
| **Sampling Rate:** | 256 kHz max per channel, programmable |
| **Data Buffering/Triggering:** | See Operations Manual for details. |
| **Bandwidth:** | 20 kHz per channel |
| **Group Delay:** | 144 µs (based on 250 kHz sampling rate)<br>(time for data sample to propagate to data register) |
| **Programmable Filter:** | Each channel incorporates an anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 128 kHz in 1 Hz steps). |
| **Common Mode Rejection:** | 70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 kHz. |
| **Common Mode Voltage:** | Signal voltage plus Common mode voltage is 10.5 volts.<br>**Note:** A/D differential inputs must not "float". Input source must have return path to ground. |
| **Output Logic:** | Bipolar output in two's complement.<br>Bipolar output range from FF80 0000 max. negative;<br>007F FFFF is max. positive (FS)<br>Unipolar output range from 0 to 00FF FFFF (FS) |
| **ESD Protection:** | Designed to meet the testing requirements of IEC 801-2 Level 2<br>(4 KV transient with a peak current of 7.5 A and $T_C$ of approximately 60 ns) |
| **Power:** | 5 VDC @ 100 mA typ., 150 mA max. / ±1 2VDC @ 200 mA (est. typ.) |
| **Ground:** | Channel inputs are differential, referenced to isolated module AGND,<br>isolated (250 V minimum peak isolation) from system power/ground. |
| **Weight:** | 1.5 oz. (42 g) |
| **VREF Detail** | VREF output @ 4.096 V (≤ 10 mA) |

Specifications are subject to change without notice.

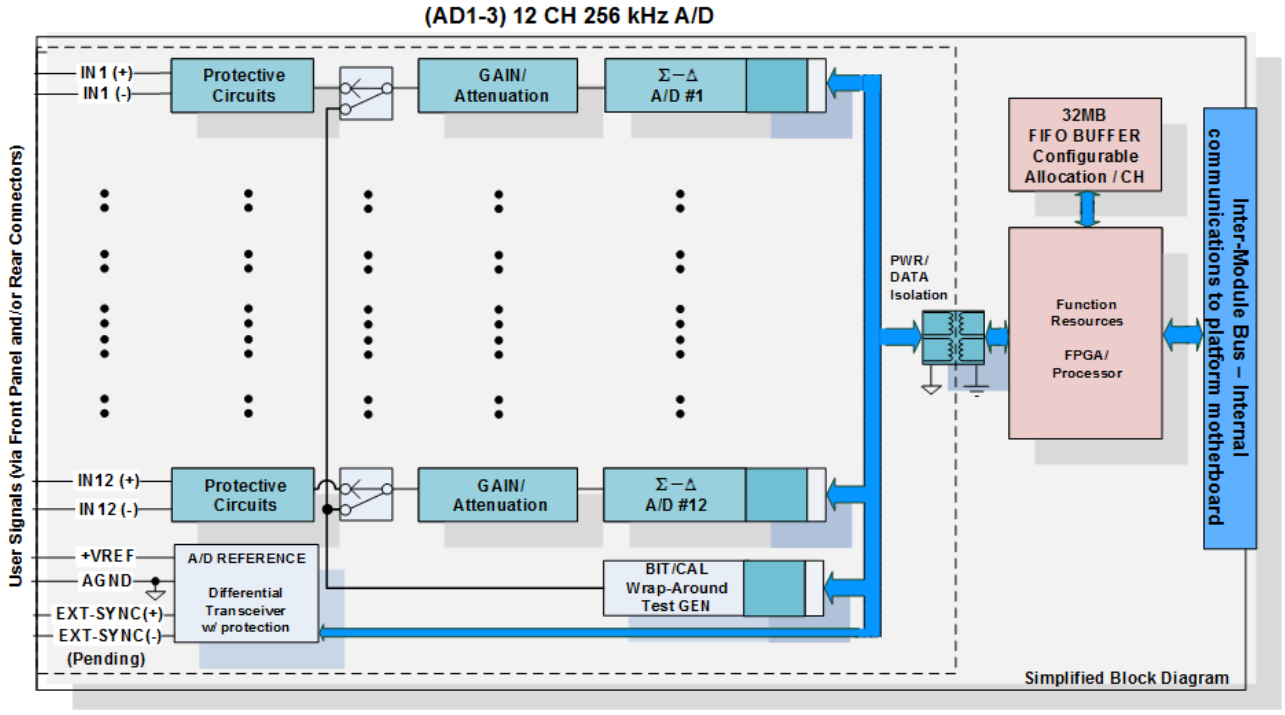
## Analog-to-Digital Module AD2 – 12 Channels (±100 to ±12.5 VDC FSR)




| | |
|---|---|
| **Resolution:** | 24-bit Sigma-Delta A/D converters. One per channel. |
| **Input Format:** | Differential voltage (may be used as single-ended by grounding one input). |
| **Input Scaling:** | Twelve (12) bipolar or unipolar channels (volts).<br>Programmable, per channel, as Full Scale (FS) range inputs of 100.00, 50.00, 25.00, or 12.50 volts where range is -FS to +FS or 0 to FS VDC. The ability to set lower voltages for FS assures the utilization of the full resolution. |
| **Overvoltage Protection:** | No damage up to ±120 V continuous; ±150 V momentary |
| **Open Input Sense:** | This module will NOT sense and report unconnected inputs. |
| **Input Impedance:** | Single Ended: 190 kΩ<br>Differential: 380 kΩ |
| **Linearity/Accuracy:** | ±0.1% FS range over temperature (voltage), to 16-bits |
| **Gain Error:** | ±0.1% FS range |
| **Offset Error:** | ±0.2% FS range |
| **Sampling Rate:** | 256 kHz max per channel, programmable |
| **Data Buffering/Triggering:** | See Operations Manual for details. |
| **Bandwidth:** | 20 kHz per channel |
| **Group Delay:** | 144 µs (based on 250 kHz sampling rate)<br>(time for data sample to propagate to data register) |
| **Programmable Filter:** | Each channel incorporates an anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 128 kHz in 1 Hz steps). |
| **Common Mode Rejection:** | 90 dB min. at 60 Hz. Roll off to 80 dB min. at 10 kHz. |
| **Common Mode Voltage:** | Signal voltage plus Common mode voltage is ±270 Volts.<br>**Note:** A/D differential inputs must not "float". Input source must have return path to ground. |
| **Output Logic:** | Bipolar output in two's complement.<br>Bipolar output range from FF80 0000 max. negative;<br>007F FFFF is max. positive (FS)<br>Unipolar output range from 0 to 00FF FFFF (FS) |
| **ESD Protection:** | Designed to meet the testing requirements of IEC 801-2 Level 2<br>(4 KV transient with a peak current of 7.5 A and $T_C$ of approximately 60 ns) |
| **Power:** | 5 VDC @ 750 mA max. |
| **Ground:** | Channel inputs are differential, referenced to isolated module AGND,<br>isolated (250 V minimum peak isolation) from system power/ground. |
| **Weight:** | 1.5 oz. (42 g) |
| **VREF Detail** | VREF output @ 4.096 V (≤ 10 mA) |

Specifications are subject to change without notice.

## Analog-to-Digital Module AD3 – 12 Channels (±25 mA FSR)




| | |
|---|---|
| **Resolution:** | 24-bit Sigma-Delta A/D converters. One per channel. |
| **Input Format:** | Differential voltage (may be used as single-ended by grounding one input). |
| **Input Scaling:** | Twelve (12) bipolar or unipolar channels (volts).<br>Programmable, per channel, as Full Scale (FS) range inputs of ± 25 mA where range is -FS to +FS or 0 to FS mA. The ability to set lower currents for FS assures the utilization of the full resolution. |
| **Overvoltage Protection:** | No damage up to ±12 V continuous; ±30 V momentary |
| **Open Input Sense:** | This module will NOT sense and report unconnected inputs. |
| **Input Impedance:** | 50 Ω min. |
| **Linearity/Accuracy:** | ±0.1% FS range over temperature (current), to 16-bits |
| **Gain Error:** | ±0.1% (current) |
| **Offset Error:** | ±0.2% FS range |
| **Sampling Rate:** | 256 kHz max per channel, programmable |
| **Data Buffering/Triggering:** | See Operations Manual for details. |
| **Bandwidth:** | 20 kHz per channel |
| **Group Delay:** | 144 µs (based on 250 kHz sampling rate)<br>(time for data sample to propagate to data register) |
| **Programmable Filter:** | Each channel incorporates an anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 128 kHz in 1 Hz steps). |
| **Common Mode Rejection:** | 70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 kHz. |
| **Common Mode Voltage:** | Signal voltage plus Common mode voltage is 10.5 volts.<br>**Note:** A/D differential inputs must not "float". Input source must have return path to ground. |
| **Output Logic:** | Bipolar output in two's complement.<br>Bipolar output range from FF80 0000 max. negative;<br>007F FFFF is max. positive (FS)<br>Unipolar output range from 0 to 00FF FFFF (FS) |
| **ESD Protection:** | Designed to meet the testing requirements of IEC 801-2 Level 2<br>(4 KV transient with a peak current of 7.5 A and $T_C$ of approximately 60 ns). |
| **Power:** | 5 VDC @ 750 mA max. |
| **Ground:** | Channel inputs are differential, referenced to isolated module AGND,<br>isolated (250 V minimum peak isolation) from system power/ground. |
| **Weight:** | 1.5 oz. (42 g) |
| **VREF Detail** | VREF output @ 4.096 V (≤ 10 mA) |

Specifications are subject to change without notice.

## Principle of Operation

Modules AD1, AD2 and AD3 are 12-channel, A/D converters. Each module contains 12, 24-Bit, Sigma-Delta A/D converters; one for each channel and an additional one for BIT. The modules provide up to 12 differential A/D channels. Inputs may be bipolar or unipolar voltages. Ranges for each module are shown below. Module AD1 will sense and report unconnected inputs. Modules AD2 and AD3 will NOT sense nor report unconnected inputs.

| Module | AD1 | AD2 | AD3 |
|---|---|---|---|
| **Full Scale Range Inputs** | 10.0 V | 100 V | NA |
| | 5.0 V | 50 V | NA |
| | 2.5 V | 25 V | NA |
| | 1.25 V | 12.5 V | NA |
| **Current Input** | NA | NA | ±25 mA |

The sample rate is programmable up to 256 kHz. Each differential channel includes an anti-aliasing filter followed by a digital “brick wall” filter and a digital second order IIR low-pass filter with a programmable breakpoint that enables users to field-adjust the filtering for each channel. The input range is field programmable for each channel. The ability to set lower voltages for Full Scale Input assures maximum resolution. All inputs are double buffered for immediate data availability. The “Latch” feature permits the user to read all A/D channels at the same time. The modules include A/D FIFO Buffering for greater control of the incoming signal (data) for analysis and display. When initialized and triggered, the A/D buffer will accept/store the data at the same rate as the base A/D sampling rate or at a lower rate when utilizing the FIFO Skip Count feature. Programmable buffer sample thresholds can be utilized for data flow control.

The module provides bipolar outputs in two’s complement with a range from FF80 0000 (maximum negative) to 007F FFFF (maximum positive). Unipolar output range is from 0 to 00FF FFFF (FS).

## Built-In Test (BIT)/Diagnostic Capability

Three different tests, one online (D2) and two off-line (D0, D3), can be selected:

The online (D2) test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus. In addition, all channels are monitored for open input on Module AD1.

The off-line (D3) test starts an initiated BIT test that disconnects all A/D’s from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 20 seconds and results can be read from the Status registers when D3 changes from **1** to **0**. The test can be stopped at any time and requires no user programming. It can be enabled or disabled via the bus. A/D Open Circuit monitoring is disabled during D3 testing.

An off-line (D0) test is used to check the card and interface. Write **1** to D0 of *Test Enable* register to disconnect all A/D channels from the I/O and to connect them across an internal D/A. Test parameters are controlled by the user and are entered in the *D0 Test Voltage* and *D0 Test Range* registers. The outputs from the A/D channels are compared to the internal D/A for proper conversion. External reference voltage is not required.

## Register Descriptions

The register descriptions provide the register name, Register Offset, Type, Data Range, Read or Write information, Initialized Value, a description of the function and, in most cases, a data table.

## A/D Reading

**Function:** Reads either voltage or current depending on mode.

**Type:** binary word (32-bit)

**Data Rage:** Unipolar: 0x0000 0000 to 0x00FF FFFF, Bipolar: 0xFF80 0000 to 0x007F FFFF

**Read/Write:** R

**Initialized Value:** NA

**Operational Settings:** Two's complement format for bipolar mode; 0x 007F FFFF=+FS, 0xFF80 0000 =-FS. For unipolar mode, range is from 0x0000 0000 to 0x00FF FFFF = FS.

## Polarity & Range

**Function:** Sets input format for polarity and range for each channel.

**Type:** binary word (32-bit)

**Data Range:** NA

**Read/Write:** R/W

**Initialized Value:** 0x0000 0010

**Operational Settings:** For bipolar/unipolar selection, program D4 as 0 for unipolar and 1 for bipolar. D1:D0 select the full scale range where b"00" is the largest range and b"11" is the smallest.

| Polarity & Range | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format input for range and polarity. | **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| Format input for range and polarity. | **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| | X | X | X | X | X | X | X | X | X | X | X | **D** | X | X | **D** | **D** |

| **Module** | **AD1** | **AD2** | **AD3** | **D1:D0** |
|---|---|---|---|---|
| **Full Scale Range Inputs*** | 10.0 V | 100 V | NA | b"00" |
| | 5.0 V | 50 V | NA | b"01" |
| | 2.5 V | 25 V | NA | b"10" |
| | 1.25 V | 12.5 V | NA | b"11" |
| **Current Input** | NA | NA | ±25 mA | b"00" |

***Note**: Each of these Full-Scale Ranges can be unipolar or bipolar.

### Filter Break Frequency

**Function:** The break frequency is the 3dB point of a digital, second-order, IIR low-pass filter.

**Type:** binary word (32-bit)

**Data Range:** NA

**Read/Write**: R/W

**Initialized Value:** AD1**:**0x0000 0000, AD2: 0x0000 4E20 (20 kHz), AD3: 0x0000 03E8 (1 kHz)

**Operational Settings:** Enter desired frequency for each channel between 10 Hz to 115.2 kHz as a 32-bit binary number (1 Hz LSB). The break frequency must not be less than 1% of the sample rate nor greater than 45% of the sample rate. For a sample rate of 2 kHz, the File Break Frequency should be no less than 20 Hz and no greater than 0.9 kHz. **0** disables filter.

### Latch All A/Ds

**Function:** Latches all channels.

**Type:** binary word (32-bit)

**Data Range:** 0x0000 0000 to 0x0000 0001

**Read/Write:** R/W

**Initialized Value:** 0

**Operational Settings:** Write **1** to D0 of *Latch All A/D* register to latch all channels. Write **0** to unlatch all channels.

**Notes:** A/D channels are latched at the current simultaneously sampled data.

### Threshold Programming

There are two thresholds that can be independently programmed on the AD1-3 modules. These thresholds are used to monitor the acquired data and set a status when the specified thresholds are reached. A configurable hysteresis may also be set to determine when the *Threshold Detect* registers are cleared. The threshold detection can be configured as a FIFO trigger to capture data based on a specified event.

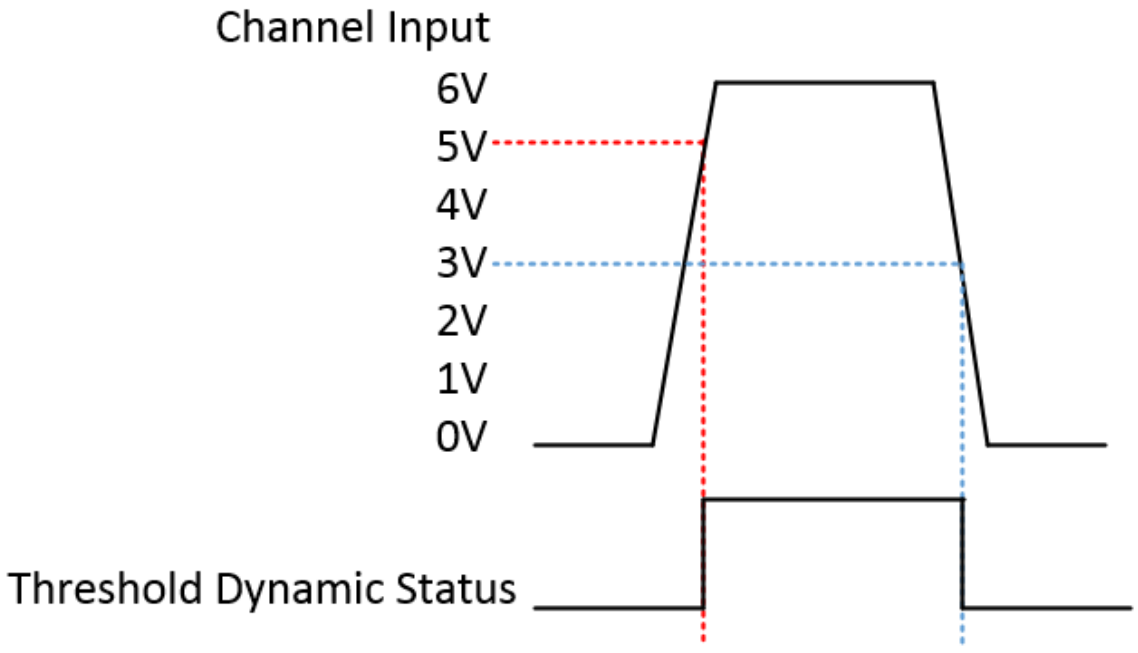



**Figure 1 - Threshold Detect programmed for a 5 V rising edge with 2 V hysteresis**

### *Threshold Detect 1*

**Function:** Sets the first threshold value.
**Type:** binary word (32-bit)
**Data Range:** 0x80 0000 to 0xFF FFFF
**Read/Write:** R/W
**Initialized Value:** 0x73 3332

| Threshold Detect 1 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| X | X | X | X | X | X | X | X | D | D | D | D | D | D | D | D |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D |

### *Threshold Detect 1 Control*

**Function:** Sets up controls to detect the first threshold.
**Type:** binary word (32-bit)
**Data Range:** 0x80 0000 to 0x1FF FFFF
**Read/Write:** R/W
**Initialized Value:** 0
**Operational Settings: D24** = Direction control; 0 = Rising, 1 = Falling. **D[23:0]** = Hysteresis amount.

| Threshold Detect 1 Control | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| X | X | X | X | X | X | X | D | D | D | D | D | D | D | D | D |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D |

### *Threshold Detect 2*

**Function:** Sets the second threshold value.
**Type:** binary word (32-bit)
**Data Range:** 0x80 0000 to 0xFF FFFF
**Read/Write:** R/W
**Initialized Value:** 0x8C CCCE

| Threshold Detect 2 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 |
| X | X | X | X | X | X | X | X | D | D | D | D | D | D | D | D |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D |

### *Threshold Detect 2 Control*

**Function:** Sets up controls to detect the second threshold.
**Type:** binary word (32-bit)
**Data Range:** 0x80 0000 to 0x1FF FFFF
**Read/Write:** R/W
**Initialized Value: 0x0100 0000**
**Operational Settings: D24** = Direction control; 0 = Rising, 1 = Falling. **D[23:0]** = Hysteresis amount.

| Threshold Detect 2 Control | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |

### D0 Polarity

**Function:** Specifies polarity of the test generator going into all channels when **D0** mode is enabled.
**Type:** binary word (32-bit)
**Data Range:** 0x0000 0000 to 0x0000 0010
**Read/Write:** R/W
**Initialized Value:** 0x0000 0000
**Operational Settings:** Write **0** to D4 of register to set channels for unipolar. Write **1** to set all channels for bipolar

| D0 Polarity | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | X | X | X | X | X | X | X | **D** | X | X | X | X |

* For bipolar/unipolar selection, program D4 as **0** for unipolar and **1** for bipolar.

### D0 Test Voltage

**Function:** Specifies voltage of the test generator going into all channels when **D0** mode is enabled.

**Type:** binary word (32-bit)

**Data Range:** See Operational Settings.

**Read/Write:** R/W

**Initialized Value:** 0x00000000

**Operational Settings:** If using bi-polar mode, write the sign extended 16-bit two's complement word (00007FFFh=+FS, FFFF8000h=-FS). If using unipolar mode, write 16-bit binary word (range: 00000000 to 0000FFFFh=FS). See *D0 Polarity* register.

**Notes:**

- If using unipolar mode with 10 V range (no other ranges), enter 00008000h for 5 V test voltage (half-scale test voltage).
- If using bipolar mode with 10 V range (no other ranges), enter 00004000h for 5 V test voltage (positive half-scale voltage). Enter FFFFC000h for –5 V (negative half-scale voltage).
- Voltages should be measured after writing words. This is true for bipolar or unipolar modes.
- The range is fixed to the largest range of the module type.

## FIFO Registers

### *FIFO Buffer Data (per channel)*

**Function:** Available data in the FIFO buffer can be retrieved, one word at a time (24 bits sign extended up to 32 bits)

**Type:** binary word (32-bit)

**Data Range:** Unipolar: 0x0000 0000 to 0x00FF FFFF, Bipolar: 0xFF80 0000 to 0x007F FFFF.

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings:** The data is presented depending upon how the *Polarity and Range* register is set, (either unipolar or bipolar).

### *FIFO Word Count*

**Function:** This is a counter that reports the number of 24-bit words stored in the FIFO buffer.

**Type:** binary word (32-bit)

**Data Range:** 0 to 0x000F FFFF

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings:** Every time a read operation is made from the FIFO Buffer Data, its corresponding *Words in FIFO* counter will be decremented by one. The maximum number of words that can be stored in the FIFO is 1 Mega words

### *FIFO E Mark*

**Function:** Marks the value when the *FIFO Buffer Data* register is almost empty.

**Type:** binary word (32-bit)

**Data Range:** NA

**Read/Write:** R/W

**Initialized Value:** 0

**Operational Settings:** When the *FIFO Word Count* register is less than or equal to the value stored in the *FIFO E Mark* register, this status is enabled.
Set = logical **1**
Reset = logical **0**

### *FIFO F Mark*

**Function:** Marks the value when the *FIFO Buffer Data* register is almost full.

**Type:** binary word (32-bit)

**Data Range:** NA

**Read/Write:** R/W

**Initialized Value:** 0

**Operational Settings:** When the *FIFO Word Count* register is greater than or equal to the value stored in the *FIFO F Mark* register, this status is enabled.
Set = logical **1**
Reset = logical **0**

### *FIFO Lo Mark*

**Function:** Marks the value when the *FIFO Buffer Data* register is at the low watermark value.

**Type:** binary word (32-bit)

**Data Range:** NA

**Read/Write:** R/W

**Initialized Value:** 0

**Operational Settings:** When the *FIFO Word Count* register is less than or equal to the value stored in the *FIFO Lo Mark* register, this status is enabled.
Set = logical **1**
Reset = logical **0**

### *FIFO Hi Mark*

**Function:** Marks the value when the *FIFO Buffer Data* register is almost full.

**Type:** binary word (32-bit)

**Data Range:** NA

**Read/Write:** R/W

**Initialized Value:** 0

**Operational Settings:** When the *FIFO Word Count* register is greater than or equal to the value stored in the *FIFO Hi Mark* register, this status is enabled.
Set = logical **1**
Reset = logical **0**

### *FIFO Buffer Delay (per channel)*

**Function:** Sets the number of delay samples before the actual FIFO data collection begins.

**Data Range:** 0x0000 0000 to 0x FFFF FFFF

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** The data sampled during the delay period will be discarded and the *FIFO Buffer Delay* register will decrement as each sample comes in until it reaches 0.

### *FIFO Buffer Size (per channel)*

**Function:** Sets the number of samples to be taken and placed into the FIFO when a trigger occurs.

**Data Range:** 0 to 0x000F FFFF

**Read/Write:** R/W

**Initialized Value:** 0x000F FFFF

**Operational Settings:** The size of each sample (number of words written to the FIFO per sample) is determined by the sample format described by the *FIFO Buffer Control* register (see *FIFO Buffer Control* register for more info).

**Notes:** The FIFO full status will only be set when the FIFO count reaches 0x000F FFFF and the “sample done” (B6) status indicates that the FIFO buffer size was reached.

### *Skip Count (per channel)*

**Function:** Sets how many samples to skip over when storing data in FIFO.

**Data Range:** 0x0000 0000 to 0xFFFF FFFF

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** If the sample rate for a channel is 10 kHz, there would be a new sample every 100µs. By setting the FIFO skip count to 1, the FIFO will store a new sample every 200 µs, or at a 5 kHz rate.

### *Clear FIFO (per channel)*

**Function:** Clears FIFO whenever clear memory is set or reset for the individual channel.

**Data Range:** 0x0000 0000 to 0x0000 0001

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** It initializes the *Words in FIFO* to zero; *Clear FIFO* register does not clear data in the buffer. A read to the buffer data will give “aged” data.

### *FIFO Buffer Control (per channel)*

**Function:** Sets the format (data type and timestamp) of the samples to be stored in the FIFO buffer which is determined by the following bitmapped table:

| | |
|---|---|
| D0 | Reserved |
| D1 | Reserved |
| D2 | Data Type. 0 = Raw (unfiltered); 1 = Filtered. |
| D3 | Reserved |
| D4 | Timestamp. An integer counter that counts from 0 to 4,294,967,295 and wraps around when it overflows. |
| D5 | Reserved |
| D6 | Reserved |
| D7 | Reserved |

**Data Range:** 0x0000 0000 to 0x000 000FF

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** Timestamp data format (D4) requires one word of storage space from the FIFO buffer. For example, if (D4) is set to **1** and data is sampled, it will store two words into the FIFO. First the sampled data followed by the timestamp. If the FIFO size is reached, any additional words (sampled data or timestamp) will be discarded. If a Filter Break Frequency is configured, setting D2 to a **1** will store the filtered data.

| **FIFO Buffer Control (per channel)** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | X | X | X | X | X | X | X | **D4** | X | **D2** | X | X |

## *FIFO Trigger Control (per channel)*

**Function:** Sets up FIFO trigger. FIFO can be started/triggered by different sources.
**Data Range:** 0x0 to 0xFFFF
**Read/Write:** R/W
**Initialized Value: 0**
**Operational Settings:** For the current implementation, triggering of FIFO is by Software Trigger or Threshold Feature. Hardware triggering will be implemented in a future release. Hardware triggering will be platform dependent based on pin-outs and I/O availability. See the tables that follow for the current and pending settings.
**Note:** The trigger must be disabled to prevent data being stored. This is true even if the FIFO is at the maximum size.

| D[1..0] | Trigger Mode |
|---|---|
| 0 | Continuous |
| 1 | Single Sample |

| D[6..4] | Trigger Type |
|---|---|
| 0 | Hardware Pos Edge (pending) |
| 1 | Hardware Neg Edge (pending) |
| 2 | Hardware Either Edge (pending) |
| 3 | Software Trigger |
| 4 | Threshold 1 |
| 5 | Threshold 2 |
| 6 | Threshold 1 or 2 |

| D8 | Trigger Enable |
|---|---|
| 0 | Not Enabled / Stop Trigger |
| 1 | Enable Trigger |

| D[15..12] | Threshold Channel Selected |
|---|---|
| 0 | Channel 1 |
| 1 | Channel 2 |
| 2 | Channel 3 |
| 3 | Channel 4 |
| 4 | Channel 5 |
| 5 | Channel 6 |
| 6 | Channel 7 |
| 7 | Channel 8 |
| 8 | Channel 9 |
| 9 | Channel 10 |
| 10 | Channel 11 |
| 11 | Channel 12 |

| D[15..0] | Examples |
|---|---|
| 0x0100 | store continuously once there is a positive edge on the Hardware Trigger |
| 0x0101 | store single sample once there is a positive edge on the Hardware Trigger |
| 0x0110 | store continuously once there is a negative edge on the Hardware Trigger |
| 0x0111 | store single sample once there is a negative edge on the Hardware Trigger |
| 0x0120 | store continuously once there is a positive or negative edge on the Hardware Trigger |
| 0x0121 | store single sample once there is a positive or negative edge on the Hardware Trigger |
| 0x0130 | store continuously once there is a Software Trigger |
| 0x0131 | store single sample once there is a Software Trigger |
| 0x1140 | store continuously once threshold 1 for channel 2 occurs |
| 0xE161 | store single sample once either threshold 1 or 2 for channel 15 occurs |
| 0x0000 | Disable Trigger (will stop FIFO from storing data if continuously running) |

## *Software Trigger*

**Function:** Software trigger is used to kick start the FIFO buffer and the collection of data.
**Data Range:** 0x0000 0000 to 0x0000 0001
**Read/Write:** R/W
**Initialized Value: 0**
**Operational Settings:** To use this operation, the *FIFO Trigger Control* register must be set up as described in the *FIFO Trigger Control* register. Write a “0x1” to trigger FIFO collection for all channels.

### Reset Timestamp

**Function:** Resets the timestamp for the FIFO.
**Data Range:** 0x0000 to 0x0001
**Read/Write:** R/W
**Initialized Value:** 0
**Operational Settings:** Write to this register to reset the timestamp.

| Reset Timestamp | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | D=DATA BIT |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **D** | D=DATA BIT |

### Sample Rate

**Function:** Single 32-bit register that sets the desired sample rate for the Active Channels.
**Data Range:** 0x3E8 to 0x3E800
**Read/Write:** R/W
**Initialized Value:** 0x186A0
**Operational Settings:** Programmable sample rates from 1 kHz up to 256 kHz for each channel.

| Sample Rate | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | D=DATA BIT |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | LSB=1Hz=DATA BIT=D |

### Test Enable

**Function:** Sets bit to enable the associated Built-In Self-Test (BIST) D3, D2, or D0.

**Data Range:** 0x0-0xF

**Read/Write:** R/W

**Initialized Value:** 0x4

**Operational Settings:** Write **1** to D2 to initiate automatic background BIT testing. The module will (every 1 second) write 55h to the *Test (D2) Verify* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) Verify* register again, after 1 second, to verify that background BIT testing is activated. D3 test cycle is completed within 20 seconds (depending on sample rate) and results can be read from the associated status registers when D3 changes from **1** to **0**. Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing **1** or terminated by writing **0**.

The on-line **(D2)** test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS range. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the appropriate register. In addition, all channels are monitored for open input on Module AD1

The off-line **(D3)** test starts an initiated BIT test that disconnects all A/D's from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS range and monitored for open inputs (AD1 only). Test cycle is completed within 20 seconds and results can be read from the *Status* registers when D3 changes from **1** to **0**. The test can be enabled or disabled at any time by writing to the appropriate register.

An off-line **(D0)** test is used to check the card and interface. Write **1** to D0 of the *Test Enable* register to disconnect all A/D channels from the I/O and to connect them across an internal D/A. Test parameters are controlled by the user and are entered in the D0 *Test Voltage* and D0 *Test Polarity* registers. The outputs from the A/D channels are monitored internally for proper conversion. External reference voltage is not required.

| Test Enabled | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | X | X | X | X | X | X | X | X | **D3** | **D2** | X | **D0** |

**The (D0) Test** is used to check the module and the interface. All channels are disconnected from the outside world, allowing the user to write any voltage to all channels on the card and then to read the data from the interface.

### Test (D2) Verify

**Function:** The module will write 55h at *Test (D2) Verify* register when (D2) is enabled (maximum one second).

**Data Range:** 0x00 or 0x55

**Read/Write:** R/W

**Initialized Value:** 0x00

**Operational Settings:** User can clear to 00h and then read again, after approximately one second, to verify that background bit testing is activated.

## Status and Interrupt Registers

The registers may be set for any or all channels and will latch if a transition is detected on a channel or channels. Each channel(s) will remain latched until the channel is cleared. Multiple channels may be cleared simultaneously, if desired. Each channel bit in the register is polled for a read status. Any subsequent channel(s) transition, if detected, will propagate through to be read (rolling-latch).

Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel) location (bit mapped per channel), will "clear" the bit (set the bit to **0**) if the actual interruptible event condition has cleared. If the interruptible condition "event" is still persistent while clearing, this may retrigger the interrupt.

There is a corresponding Interrupt Enable and vector associated with each "Latched" Status. Each status type may be "polled" (at any time), or is "interruptible" when interrupts are enabled and the associated Interrupt Service Routine (ISR) vectors are programmed accordingly. When programmed for "interruptible" status, interrupts are typically generated and flagged with the programmed vector available as data. The host or single board computer (SBC) typically services the interrupt by a general or specific ISR, which reads the (typically) unique programmed vector (identifier of which status generated the interrupt), reads the associated status register to determine which channel in the status register was "flagged" and then "clears" the status register. This essentially resets the interrupt mechanism, which is now ready to be triggered by the next status register detected event "flag". "Latched Status" will trigger on either "sense on edge" or "sense on level" based on the settings of the associated Set Edge/Level Interrupt register. Sense on "edge" requires a change from low to high state to trigger the status detection, while sense on "level" is independent of the previous state. Unless otherwise specified, all status or fault indications are bit set per channel.

### BIT Dynamic Status

**Function:** Continuously reports the status of the Built In Self Tests.

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Non-compliant A/D conversion (outside 0.2% FS range accuracy spec).

**Notes:** BIT Status is part of background testing and the status register may be checked or polled at any given time.

| BIT Dynamic Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## BIT Latched Status

**Function:** Latches high when there's a non-compliant status until cleared.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Non-compliant A/D conversion (outside 0.2% FS range accuracy spec). Write a **1** to this register to clear status.

**Notes:** BIT Status is part of background testing and the status register may be checked or polled at any given time.

| BIT Latched Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## BIT Interrupt Enable

**Function:** Enables interrupts for the BIT Status

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** When enabled, a non-compliant channel will trigger an interrupt.

| BIT Interrupt Enable | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## BIT Set Edge/Level Interrupt

**Function:** When the *BIT Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either "sense on edge" or "sense on level" event detection.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** Write a **1** to sense on level and a **0** to sense on edge.

| BIT Set Edge/Level Interrupt | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## FIFO Dynamic Status

**Function:** Checks the corresponding bit for a channel's FIFO Status. The *FIFO Dynamic Status* register indicates the current condition of the FIFO buffer.

**Type:** binary word (32-bit)

**Data Range:** 0 to 0x0000 007F

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings: D0**-**D6** is used to show the different conditions of the buffer.

| Description | | Configurable? |
|---|---|---|
| **D0** | Empty; 1 when FIFO Count = 0 | No |
| **D1** | Almost Empty; 1 when FIFO Count <= AE register | Yes |
| **D2** | Low Watermark; 1 when FIFO Count <= LWM register | Yes |
| **D3** | High Watermark; 1 when FIFO Count >= HWM register | Yes |
| **D4** | Almost Full; 1 when FIFO Count >= AF register | Yes |
| **D5** | Full; 1 when FIFO Count = 1 Mega Words (2 M pending) | No |
| **D6** | Sample Done; 1 when FIFO Count "FIFO Buffer Size" register | Yes |

| FIFO Dynamic Status | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | D=DATA BIT |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | **D** | **D** | **D** | **D** | **D** | **D** | **D** | D=DATA BIT |

## FIFO Latched Status

**Function:** Checks the corresponding bit for a channel's FIFO Status. The *FIFO Latched Status* register maintains the last condition of the FIFO buffer, until cleared.

**Type:** binary word (32-bit)

**Data Range:** 0 to 0x0000 007F

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings: D0**-**D6** is used to show the different conditions of the buffer. Write a **1** to this register to clear status.

| Description | | Configurable? |
|---|---|---|
| **D0** | Empty; 1 when FIFO Count = 0 | No |
| **D1** | Almost Empty; 1 when FIFO Count <= AE register | Yes |
| **D2** | Low Watermark; 1 when FIFO Count <= LWM register | Yes |
| **D3** | High Watermark; 1 when FIFO Count >= HWM register | Yes |
| **D4** | Almost Full; 1 when FIFO Count >= AF register | Yes |
| **D5** | Full; 1 when FIFO Count = 1 Mega Words (2 M pending) | No |
| **D6** | Sample Done; 1 when FIFO Count "FIFO Buffer Size" register | Yes |

| FIFO Latched Status | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | D=DATA BIT |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | **D** | **D** | **D** | **D** | **D** | **D** | **D** | D=DATA BIT |

## FIFO Status Interrupt Enable

**Function:** Set the corresponding channel bit to enable an interrupt for each of the conditions indicated in the FIFO Status register (B0-B6).

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** When enabled, an interrupt will be generated for each of the following conditions. Each channel may be set for a different condition.

| Description | |
|---|---|
| **D0** | Empty; 1 when FIFO Count = 0 |
| **D1** | Almost Empty; 1 when FIFO Count <= AE register |
| **D2** | Low Watermark; 1 when FIFO Count <= LWM register |
| **D3** | High Watermark; 1 when FIFO Count >= HWM register |
| **D4** | Almost Full; 1 when FIFO Count >= AF register |
| **D5** | Full; 1 when FIFO Count = 1 Mega Words (2 M pending) |
| **D6** | Sample Done; 1 when FIFO Count "FIFO Buffer Size" register |

| FIFO Status Interrupt Enable | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | D=DATA BIT |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | **D** | **D** | **D** | **D** | **D** | **D** | **D** | D=DATA BIT |

## FIFO Set Edge/Level Interrupt

**Function:** When the *FIFO Status Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** Write a **1** to sense on level and a **0** to sense on edge.

| FIFO Set Edge/Level Interrupt | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | D=DATA BIT |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| X | X | X | X | X | X | X | X | X | **D** | **D** | **D** | **D** | **D** | **D** | **D** | D=DATA BIT |

## Overcurrent Dynamic Status

**Function:** Continuously reports the overcurrent status of each channel.

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Overcurrent

| Overcurrent Dynamic Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## Overcurrent Latched Status

**Function:** Latches high when an overcurrent condition occurs until cleared.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Overcurrent. Write a **1** to this register to clear status.

| Overcurrent Latched Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## Overcurrent Interrupt Enable

**Function:** Set the corresponding channel bit to enable an interrupt for an overcurrent condition.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** When enabled, a non-compliant channel will trigger an interrupt.

| Overcurrent Interrupt Enable | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## Overcurrent Set Edge/Level Interrupt

**Function:** When the *Overcurrent Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** Write a **1** to sense on level and a **0** to sense on edge.

| Overcurrent Set Edge/Level Interrupt | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## Open Dynamic Status

**Function:** Continuously reports the status of the open detect for each channel. Only applicable to the AD1 and only when the AD1 is set for voltage measurement mode.

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Open Status

| Open Dynamic Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

## Open Latched Status

**Function:** Latches high when an open condition occurs until cleared. Only applicable to the AD1 and only when the AD1 is set for voltage measurement mode.

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Open Status Write a **1** to this register to clear status.

| Open Latched Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

## Open Status Interrupt Enable

**Function:** Set the corresponding channel bit to enable an interrupt for an open status condition. Only applicable to the AD1 and only when the AD1 is set for voltage measurement mode.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** When enabled, a non-compliant channel will trigger an interrupt.

| Open Status Interrupt Enable | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

## Open Status Set Edge/Level Interrupt

**Function:** When the *Open Status Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection. Only applicable to the AD1 and only when the AD1 is set for voltage measurement mode.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** Write a **1** to sense on level and a **0** to sense on edge.

| Open Status Set Edge/Level Interrupt | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo | Hi | Lo |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

## Threshold Dynamic Status

**Function:** Continuously reports the status of the two threshold detects for each channel.

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Outside of threshold range. The status is created based on the values set in the *Threshold Detect 1* and *Threshold Detect 2* registers. Bits **D0** and **D1** represent if channel 1 is outside the threshold for *Threshold Detect 1* and *Threshold Detect 2* respectively, Bits **D2** and **D3** represent if channel 2 is outside the threshold for *Threshold Detect 1* and *Threshold Detect 2* respectively, etc. This pattern continues for all channels.

| Threshold Dynamic Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

### Threshold Latched Status

**Function:** Latches high when a threshold detect condition occurs until cleared.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Outside of threshold range. The status is created based on the values set in the *Threshold Detect 1* and *Threshold Detect 2* registers. Bits **D0** and **D1** represent if channel 1 is outside the threshold for *Threshold Detect 1* and *Threshold Detect 2* respectively, Bits **D2** and **D3** represent if channel 2 is outside the threshold for *Threshold Detect 1* and *Threshold Detect 2* respectively, etc. This pattern continues for all channels. Write a **1** to this register to clear status.

| Threshold Latched Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

### Threshold Interrupt Enable

**Function:** Sets the corresponding channel bit to enable interrupts for the corresponding channel.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** When enabled, a non-compliant channel will trigger an interrupt.

| Threshold Interrupt Enable | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

### Threshold Set Edge/Level Interrupt

**Function:** When the *Threshold Status Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** Write a **1** to sense on level and a **0** to sense on edge.

| Threshold Set Edge/Level Interrupt | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | Ch.12 | | Ch.11 | | Ch.10 | | Ch.9 | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| Ch.8 | | Ch.7 | | Ch.6 | | Ch.5 | | Ch.4 | | Ch.3 | | Ch.2 | | Ch.1 | |

## Frontend Amplifier Failure Dynamic Status

**Function:** Continuously reports the frontend amplifier status for each channel. This register only applies to AD1.

**Read/Write:** R

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Frontend amplifier failure.

| Frontend Amplifier Failure Dynamic Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## Frontend Amplifier Failure Latched Status

**Function:** Latches high when a frontend amplifier failure is detected until cleared. This register only applies to AD1.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings: 0** = Normal; **1** = Frontend amplifier failure. Write a **1** to this register to clear status.

| Frontend Amplifier Failure Latched Status | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## Frontend Amplifier Failure Interrupt Enable

**Function:** Set the bit to enable interrupts for the corresponding channel. This register only applies to AD1.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** When enabled, a non-compliant channel will trigger an interrupt.

| Frontend Amplifier Failure Interrupt Enable | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

### Frontend Amplifier Failure Set Edge/Level Interrupt

**Function:** When the *Frontend Amplifier Failure Interrupt Enable* register is enabled, this register determines whether the interrupt will be generated for either “sense on edge” or “sense on level” event detection. This register only applies to AD1.

**Read/Write:** R/W

**Initialized Value: 0**

**Operational Settings:** Write a **1** to sense on level and a **0** to sense on edge.

| Frontend Amplifier Failure Set Edge/Level Interrupt | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| X | X | X | X | Ch.12 | Ch.11 | Ch.10 | Ch.9 | Ch.8 | Ch.7 | Ch.6 | Ch.5 | Ch.4 | Ch.3 | Ch.2 | Ch.1 |

## Function Register Map

| | | |
|---|---|---|
| 0x1000 | A/D Reading Ch. 1 | R |
| 0x1004 | A/D Reading Ch. 2 | R |
| 0x1008 | A/D Reading Ch. 3 | R |
| 0x100C | A/D Reading Ch. 4 | R |
| 0x1010 | A/D Reading Ch. 5 | R |
| 0x1014 | A/D Reading Ch. 6 | R |
| 0x1018 | A/D Reading Ch. 7 | R |
| 0x101C | A/D Reading Ch. 8 | R |
| 0x1020 | A/D Reading Ch. 9 | R |
| 0x1024 | A/D Reading Ch. 10 | R |
| 0x1028 | A/D Reading Ch. 11 | R |
| 0x102C | A/D Reading Ch. 12 | R |

| | | |
|---|---|---|
| 0x1080 | Polarity & Range Ch.1 | R/W |
| 0x1084 | Polarity & Range Ch.2 | R/W |
| 0x1088 | Polarity & Range Ch.3 | R/W |
| 0x108C | Polarity & Range Ch.4 | R/W |
| 0x1090 | Polarity & Range Ch.5 | R/W |
| 0x1094 | Polarity & Range Ch.6 | R/W |
| 0x1098 | Polarity & Range Ch.7 | R/W |
| 0x109C | Polarity & Range Ch.8 | R/W |
| 0x10A0 | Polarity & Range Ch.9 | R/W |
| 0x10A4 | Polarity & Range Ch.10 | R/W |
| 0x10A8 | Polarity & Range Ch.11 | R/W |
| 0x10AC | Polarity & Range Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1100 | Filter Break Freq Ch.1 | R/W |
| 0x1104 | Filter Break Freq Ch.2 | R/W |
| 0x1108 | Filter Break Freq Ch.3 | R/W |
| 0x110C | Filter Break Freq Ch.4 | R/W |
| 0x1110 | Filter Break Freq Ch.5 | R/W |
| 0x1114 | Filter Break Freq Ch.6 | R/W |
| 0x1118 | Filter Break Freq Ch.7 | R/W |
| 0x111C | Filter Break Freq Ch.8 | R/W |
| 0x1120 | Filter Break Freq Ch.9 | R/W |
| 0x1124 | Filter Break Freq Ch.10 | R/W |
| 0x1128 | Filter Break Freq Ch.11 | R/W |
| 0x112C | Filter Break Freq Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1180 | FIFO Buffer Data Ch. 1 | R |
| 0x1184 | FIFO Buffer Data Ch. 2 | R |
| 0x1188 | FIFO Buffer Data Ch. 3 | R |
| 0x118C | FIFO Buffer Data Ch. 4 | R |
| 0x1190 | FIFO Buffer Data Ch. 5 | R |
| 0x1194 | FIFO Buffer Data Ch. 6 | R |
| 0x1198 | FIFO Buffer Data Ch. 7 | R |
| 0x119C | FIFO Buffer Data Ch. 8 | R |
| 0x11A0 | FIFO Buffer Data Ch. 9 | R |
| 0x11A4 | FIFO Buffer Data Ch. 10 | R |
| 0x11A8 | FIFO Buffer Data Ch. 11 | R |
| 0x11AC | FIFO Buffer Data Ch. 12 | R |

| | | |
|---|---|---|
| 0x1200 | FIFO Word Count Ch. 1 | R |
| 0x1204 | FIFO Word Count Ch. 2 | R |
| 0x1208 | FIFO Word Count Ch. 3 | R |
| 0x120C | FIFO Word Count Ch. 4 | R |
| 0x1210 | FIFO Word Count Ch. 5 | R |
| 0x1214 | FIFO Word Count Ch.6 | R |
| 0x1218 | FIFO Word Count Ch.7 | R |
| 0x121C | FIFO Word Count Ch. 8 | R |
| 0x1220 | FIFO Word Count Ch. 9 | R |
| 0x1224 | FIFO Word Count Ch. 10 | R |
| 0x1228 | FIFO Word Count Ch. 11 | R |
| 0x122C | FIFO Word Count Ch. 12 | R |

| | | |
|---|---|---|
| 0x1280 | FIFO E Mark Ch. 1 | R/W |
| 0x1284 | FIFO E Mark Ch. 2 | R/W |
| 0x1288 | FIFO E Mark Ch. 3 | R/W |
| 0x128C | FIFO E Mark Ch. 4 | R/W |
| 0x1290 | FIFO E Mark Ch. 5 | R/W |
| 0x1294 | FIFO E Mark Ch. 6 | R/W |
| 0x1298 | FIFO E Mark Ch. 7 | R/W |
| 0x129C | FIFO E Mark Ch. 8 | R/W |
| 0x12A0 | FIFO E Mark Ch. 9 | R/W |
| 0x12A4 | FIFO E Mark Ch. 10 | R/W |
| 0x12A8 | FIFO E Mark Ch. 11 | R/W |
| 0x12AC | FIFO E Mark Ch. 12 | R/W |

| | | |
|---|---|---|
| 0x1300 | FIFO F Mark Ch.1 | R/W |
| 0x1304 | FIFO F Mark Ch.2 | R/W |
| 0x1308 | FIFO F Mark Ch.3 | R/W |
| 0x130C | FIFO F Mark Ch.4 | R/W |
| 0x1310 | FIFO F Mark Ch.5 | R/W |
| 0x1314 | FIFO F Mark Ch.6 | R/W |
| 0x1318 | FIFO F Mark Ch.7 | R/W |
| 0x131C | FIFO F Mark Ch.8 | R/W |
| 0x1320 | FIFO F Mark Ch.9 | R/W |
| 0x1324 | FIFO F Mark Ch.10 | R/W |
| 0x1328 | FIFO F Mark Ch.11 | R/W |
| 0x132C | FIFO F Mark Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1380 | FIFO Lo Mark Ch.1 | R/W |
| 0x1384 | FIFO Lo Mark Ch.2 | R/W |
| 0x1388 | FIFO Lo Mark Ch.3 | R/W |
| 0x138C | FIFO Lo Mark Ch.4 | R/W |
| 0x1390 | FIFO Lo Mark Ch.5 | R/W |
| 0x1394 | FIFO Lo Mark Ch.6 | R/W |
| 0x1398 | FIFO Lo Mark Ch.7 | R/W |
| 0x139C | FIFO Lo Mark Ch.8 | R/W |
| 0x13A0 | FIFO Lo Mark Ch.9 | R/W |
| 0x13A4 | FIFO Lo Mark Ch.10 | R/W |
| 0x13A8 | FIFO Lo Mark Ch.11 | R/W |
| 0x13AC | FIFO Lo Mark Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1400 | FIFO Hi Mark Ch. 1 | R/W |
| 0x1404 | FIFO Hi Mark Ch. 2 | R/W |
| 0x1408 | FIFO Hi Mark Ch. 3 | R/W |
| 0x140C | FIFO Hi Mark Ch. 4 | R/W |
| 0x1410 | FIFO Hi Mark Ch. 5 | R/W |
| 0x1414 | FIFO Hi Mark Ch. 6 | R/W |
| 0x1418 | FIFO Hi Mark Ch. 7 | R/W |
| 0x141C | FIFO Hi Mark Ch. 8 | R/W |
| 0x1420 | FIFO Hi Mark Ch. 9 | R/W |
| 0x1424 | FIFO Hi Mark Ch. 10 | R/W |
| 0x1428 | FIFO Hi Mark Ch. 11 | R/W |
| 0x142C | FIFO Hi Mark Ch. 12 | R/W |

| | | |
|---|---|---|
| 0x1480 | FIFO Buffer Delay Ch.1 | R/W |
| 0x1484 | FIFO Buffer Delay Ch.2 | R/W |
| 0x1488 | FIFO Buffer Delay Ch.3 | R/W |
| 0x148C | FIFO Buffer Delay Ch.4 | R/W |
| 0x1490 | FIFO Buffer Delay Ch.5 | R/W |
| 0x1494 | FIFO Buffer Delay Ch.6 | R/W |
| 0x1498 | FIFO Buffer Delay Ch.7 | R/W |
| 0x149C | FIFO Buffer Delay Ch.8 | R/W |
| 0x14A0 | FIFO Buffer Delay Ch.9 | R/W |
| 0x14A4 | FIFO Buffer Delay Ch.10 | R/W |
| 0x14A8 | FIFO Buffer Delay Ch.11 | R/W |
| 0x14AC | FIFO Buffer Delay Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1500 | FIFO Buffer Size Ch.1 | R/W |
| 0x1504 | FIFO Buffer Size Ch.2 | R/W |
| 0x1508 | FIFO Buffer Size Ch.3 | R/W |
| 0x150C | FIFO Buffer Size Ch.4 | R/W |
| 0x1510 | FIFO Buffer Size Ch.5 | R/W |
| 0x1514 | FIFO Buffer Size Ch.6 | R/W |
| 0x1518 | FIFO Buffer Size Ch.7 | R/W |
| 0x151C | FIFO Buffer Size Ch.8 | R/W |
| 0x1520 | FIFO Buffer Size Ch.9 | R/W |
| 0x1524 | FIFO Buffer Size Ch.10 | R/W |
| 0x1528 | FIFO Buffer Size Ch.11 | R/W |
| 0x152C | FIFO Buffer Size Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1580 | Skip Count Ch.1 | R/W |
| 0x1584 | Skip Count Ch.2 | R/W |
| 0x1588 | Skip Count Ch.3 | R/W |
| 0x158C | Skip Count Ch.4 | R/W |
| 0x1590 | Skip Count Ch.5 | R/W |
| 0x1594 | Skip Count Ch.6 | R/W |
| 0x1598 | Skip Count Ch.7 | R/W |
| 0x159C | Skip Count Ch.8 | R/W |
| 0x15A0 | Skip Count Ch.9 | R/W |
| 0x15A4 | Skip Count Ch.10 | R/W |
| 0x15A8 | Skip Count Ch.11 | R/W |
| 0x15AC | Skip Count Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1600 | Clear FIFO Ch.1 | R/W |
| 0x1604 | Clear FIFO Ch.2 | R/W |
| 0x1608 | Clear FIFO Ch.3 | R/W |
| 0x160C | Clear FIFO Ch.4 | R/W |
| 0x1610 | Clear FIFO Ch.5 | R/W |
| 0x1614 | Clear FIFO Ch.6 | R/W |
| 0x1618 | Clear FIFO Ch.7 | R/W |
| 0x161C | Clear FIFO Ch.8 | R/W |
| 0x1620 | Clear FIFO Ch.9 | R/W |
| 0x1624 | Clear FIFO Ch.10 | R/W |
| 0x1628 | Clear FIFO Ch.11 | R/W |
| 0x162C | Clear FIFO Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1680 | FIFO Buffer Control Ch.1 | R/W |
| 0x1684 | FIFO Buffer Control Ch.2 | R/W |
| 0x1688 | FIFO Buffer Control Ch.3 | R/W |
| 0x168C | FIFO Buffer Control Ch.4 | R/W |
| 0x1690 | FIFO Buffer Control Ch.5 | R/W |
| 0x1694 | FIFO Buffer Control Ch.6 | R/W |
| 0x1698 | FIFO Buffer Control Ch.7 | R/W |
| 0x169C | FIFO Buffer Control Ch.8 | R/W |
| 0x16A0 | FIFO Buffer Control Ch.9 | R/W |
| 0x16A4 | FIFO Buffer Control Ch.10 | R/W |
| 0x16A8 | FIFO Buffer Control Ch.11 | R/W |
| 0x16AC | FIFO Buffer Control Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1980 | Threshold Detect 1 Ch.1 | R/W |
| 0x1984 | Threshold Detect 1 Ch.2 | R/W |
| 0x1988 | Threshold Detect 1 Ch.3 | R/W |
| 0x198C | Threshold Detect 1 Ch.4 | R/W |
| 0x1990 | Threshold Detect 1 Ch.5 | R/W |
| 0x1994 | Threshold Detect 1 Ch.6 | R/W |
| 0x1998 | Threshold Detect 1 Ch.7 | R/W |
| 0x199C | Threshold Detect 1 Ch.8 | R/W |
| 0x19A0 | Threshold Detect 1 Ch.9 | R/W |
| 0x19A4 | Threshold Detect 1 Ch.10 | R/W |
| 0x19A8 | Threshold Detect 1 Ch.11 | R/W |
| 0x19AC | Threshold Detect 1 Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1A00 | Threshold Detect 1 Control Ch.1 | R/W |
| 0x1A04 | Threshold Detect 1 Control Ch.2 | R/W |
| 0x1A08 | Threshold Detect 1 Control Ch.3 | R/W |
| 0x1A0C | Threshold Detect 1 Control Ch.4 | R/W |
| 0x1A10 | Threshold Detect 1 Control Ch.5 | R/W |
| 0x1A14 | Threshold Detect 1 Control Ch.6 | R/W |
| 0x1A18 | Threshold Detect 1 Control Ch.7 | R/W |
| 0x1A1C | Threshold Detect 1 Control Ch.8 | R/W |
| 0x1A20 | Threshold Detect 1 Control Ch.9 | R/W |
| 0x1A24 | Threshold Detect 1 Control Ch.10 | R/W |
| 0x1A28 | Threshold Detect 1 Control Ch.11 | R/W |
| 0x1A2C | Threshold Detect 1 Control Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1A80 | Threshold Detect 2 Ch.1 | R/W |
| 0x1A84 | Threshold Detect 2 Ch.2 | R/W |
| 0x1A88 | Threshold Detect 2 Ch.3 | R/W |
| 0x1A8C | Threshold Detect 2 Ch.4 | R/W |
| 0x1A90 | Threshold Detect 2 Ch.5 | R/W |
| 0x1A94 | Threshold Detect 2 Ch.6 | R/W |
| 0x1A98 | Threshold Detect 2 Ch.7 | R/W |
| 0x1A9C | Threshold Detect 2 Ch.8 | R/W |
| 0x1AA0 | Threshold Detect 2 Ch.9 | R/W |
| 0x1AA4 | Threshold Detect 2 Ch.10 | R/W |
| 0x1AA8 | Threshold Detect 2 Ch.11 | R/W |
| 0x1AAC | Threshold Detect 2 Ch.12 | R/W |

| | | |
|---|---|---|
| 0x1B00 | Threshold Detect 2 Control Ch.1 | R/W |
| 0x1B04 | Threshold Detect 2 Control Ch.2 | R/W |
| 0x1B08 | Threshold Detect 2 Control Ch.3 | R/W |
| 0x1B0C | Threshold Detect 2 Control Ch.4 | R/W |
| 0x1B10 | Threshold Detect 2 Control Ch.5 | R/W |
| 0x1B14 | Threshold Detect 2 Control Ch.6 | R/W |
| 0x1B18 | Threshold Detect 2 Control Ch.7 | R/W |
| 0x1B1C | Threshold Detect 2 Control Ch.8 | R/W |
| 0x1B20 | Threshold Detect 2 Control Ch.9 | R/W |
| 0x1B24 | Threshold Detect 2 Control Ch.10 | R/W |
| 0x1B28 | Threshold Detect 2 Control Ch.11 | R/W |
| 0x1B2C | Threshold Detect 2 Control Ch.12 | R/W |

| | | |
|---|---|---|
| 0x16C0 | Reset Timestamp | R/W |
| 0x1880 | Latch all A/D | R/W |
| 0x1884 | FIFO Trig Control | R/W |
| 0x1888 | Software Trigger | R/W |
| 0x188C | Sample Rate | R/W |
| 0x0914 | Clear Overcurrent | R/W |
| 0x0294 | D0 Polarity | R/W |
| 0x0298 | D0 Test Voltage | R/W |
| 0x0248 | Test Enable | R/W |
| 0x024C | Test (D2) Verify | R/W |
| 0x0294 | D0 Test Value | R/W |
| 0x0298 | D0 Test Polarity | R/W |

## BIT

| | | |
|---|---|---|
| 0x0800 | Dynamic Status | R |
| 0x0804 | Latched Status | R/W |
| 0x0808 | Interrupt Enable | R/W |
| 0x080C | Set Edge/Level Interrupt | R/W |

## FIFO Status

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Ch. 1** | 0x0810 | Dynamic Status | R | **Ch. 7** | 0x0870 | Dynamic Status | R |
| | 0x0814 | Latched Status | R/W | | 0x0874 | Latched Status | R/W |
| | 0x0818 | Interrupt Enable | R/W | | 0x0878 | Interrupt Enable | R/W |
| | 0x081C | Set Edge/Level Interrupt | R/W | | 0x087C | Set Edge/Level Interrupt | R/W |
| **Ch. 2** | 0x0820 | Dynamic Status | R | **Ch. 8** | 0x0880 | Dynamic Status | R |
| | 0x0824 | Latched Status | R/W | | 0x0884 | Latched Status | R/W |
| | 0x0828 | Interrupt Enable | R/W | | 0x0888 | Interrupt Enable | R/W |
| | 0x082C | Set Edge/Level Interrupt | R/W | | 0x088C | Set Edge/Level Interrupt | R/W |
| **Ch. 3** | 0x0830 | Dynamic Status | R | **Ch. 9** | 0x0890 | Dynamic Status | R |
| | 0x0834 | Latched Status | R/W | | 0x0894 | Latched Status | R/W |
| | 0x0838 | Interrupt Enable | R/W | | 0x0898 | Interrupt Enable | R/W |
| | 0x083C | Set Edge/Level Interrupt | R/W | | 0x089C | Set Edge/Level Interrupt | R/W |
| **Ch. 4** | 0x0840 | Dynamic Status | R | **Ch. 10** | 0x08A0 | Dynamic Status | R |
| | 0x0844 | Latched Status | R/W | | 0x08A4 | Latched Status | R/W |
| | 0x0848 | Interrupt Enable | R/W | | 0x08A8 | Interrupt Enable | R/W |
| | 0x084C | Set Edge/Level Interrupt | R/W | | 0x08AC | Set Edge/Level Interrupt | R/W |
| **Ch. 5** | 0x0850 | Dynamic Status | R | **Ch. 11** | 0x08B0 | Dynamic Status | R |
| | 0x0854 | Latched Status | R/W | | 0x08B4 | Latched Status | R/W |
| | 0x0858 | Interrupt Enable | R/W | | 0x08B8 | Interrupt Enable | R/W |
| | 0x085C | Set Edge/Level Interrupt | R/W | | 0x08BC | Set Edge/Level Interrupt | R/W |
| **Ch. 6** | 0x0860 | Dynamic Status | R | **Ch. 12** | 0x08C0 | Dynamic Status | R |
| | 0x0864 | Latched Status | R/W | | 0x08C4 | Latched Status | R/W |
| | 0x0868 | Interrupt Enable | R/W | | 0x08C8 | Interrupt Enable | R/W |
| | 0x086C | Set Edge/Level Interrupt | R/W | | 0x08CC | Set Edge/Level Interrupt | R/W |

## Overcurrent

| | | |
|---|---|---|
| 0x0910 | Dynamic Status | R |
| 0x0914 | Latched Status | R/W |
| 0x0918 | Interrupt Enable | R/W |
| 0x091C | Set Edge/Level Interrupt | R/W |

## Open Status

| | | |
|---|---|---|
| 0x0920 | Dynamic Status | R |
| 0x0924 | Latched Status | R/W |
| 0x0928 | Interrupt Enable | R/W |
| 0x092C | Set Edge/Level Interrupt | R/W |

### Threshold

| | | |
|---|---|---|
| 0x0940 | Dynamic Status | R |
| 0x0944 | Latched Status | R/W |
| 0x0948 | Interrupt Enable | R/W |
| 0x094C | Set Edge/Level Interrupt | R/W |

### Frontend Amplifier Failure

| | | |
|---|---|---|
| 0x0950 | Dynamic Status | R |
| 0x0954 | Latched Status | R/W |
| 0x0958 | Interrupt Enable | R/W |
| 0x095C | Set Edge/Level Interrupt | R/W |

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# Analog-to-Digital Threshold and Saturation Programming

# A/D MODULE MANUAL APPENDIX

# Revision History

| Revision | Revision Date | Description | Draft/Apprv. |
|---|---|---|---|
| A | 7/2/2019 | Initial release | GC |
| B | 3/29/2021 | ECO C08381:<br>- Corrected manual name in footer<br>- Revised Section 3.2.2 to correct Enable/Disable Saturation<br>- Detection bit settings and add description of odd/even bits configuration<br>- Revised COSA® definition | DG/ars |

# Table of Contents

# 1 Threshold and Saturation Capability

The Threshold and Saturation Capability is available on the following modules:

- Analog-to-Digital (A/D) Modules
  - AD1 – 12 Channels Analog-to-Digital (Voltage Input Only) (±10 to ±1.25 VDC FSR)
  - AD2 – 12 Channels Analog-to-Digital (Voltage Input Only) (±100 to ±12.5 VDC FSR)
  - AD3 – 12 Channels Analog-to-Digital (Current Input Only) (±25 mA FSR)
  - AD4 – 16 Channels Analog-to-Digital (±10.0 to ±1.25 VDC or ±25 mA FSR)
  - AD5 – 16 Channels Analog-to-Digital (±50.0 to ±6.25 VDC FSR)
  - AD6 – 16 Channels Analog-to-Digital (±100 to ±12.5 VDC FSR)
  - ADE – 16 Channels Analog-to-Digital (Voltage Input Only) (±10 to ±0.625 VDC FSR)
  - ADF – 16 Channels Analog-to-Digital (Voltage Input Only) (±100 to ±6.25 VDC FSR)
  - ADG – 16 Channels Analog-to-Digital (Current Input Only) (±25 to ±12.5 mA FSR)

# 2 Principle of Operation

The AD modules provide the ability to monitor the acquired data and set a status when the specific thresholds are reached.

## 2.1 Threshold Detect

There are two thresholds that can be independently programmed on the A/D modules. These thresholds are used to monitor the acquired data and set a status when the specified thresholds are reached. A configurable hysteresis may also be set to determine when the *Threshold Detect* registers are cleared. The threshold detection can be configured as a FIFO trigger to capture data based on a specified event. Refer to Figure 1 and Figure 2 for illustrations for Threshold Detect Programming.

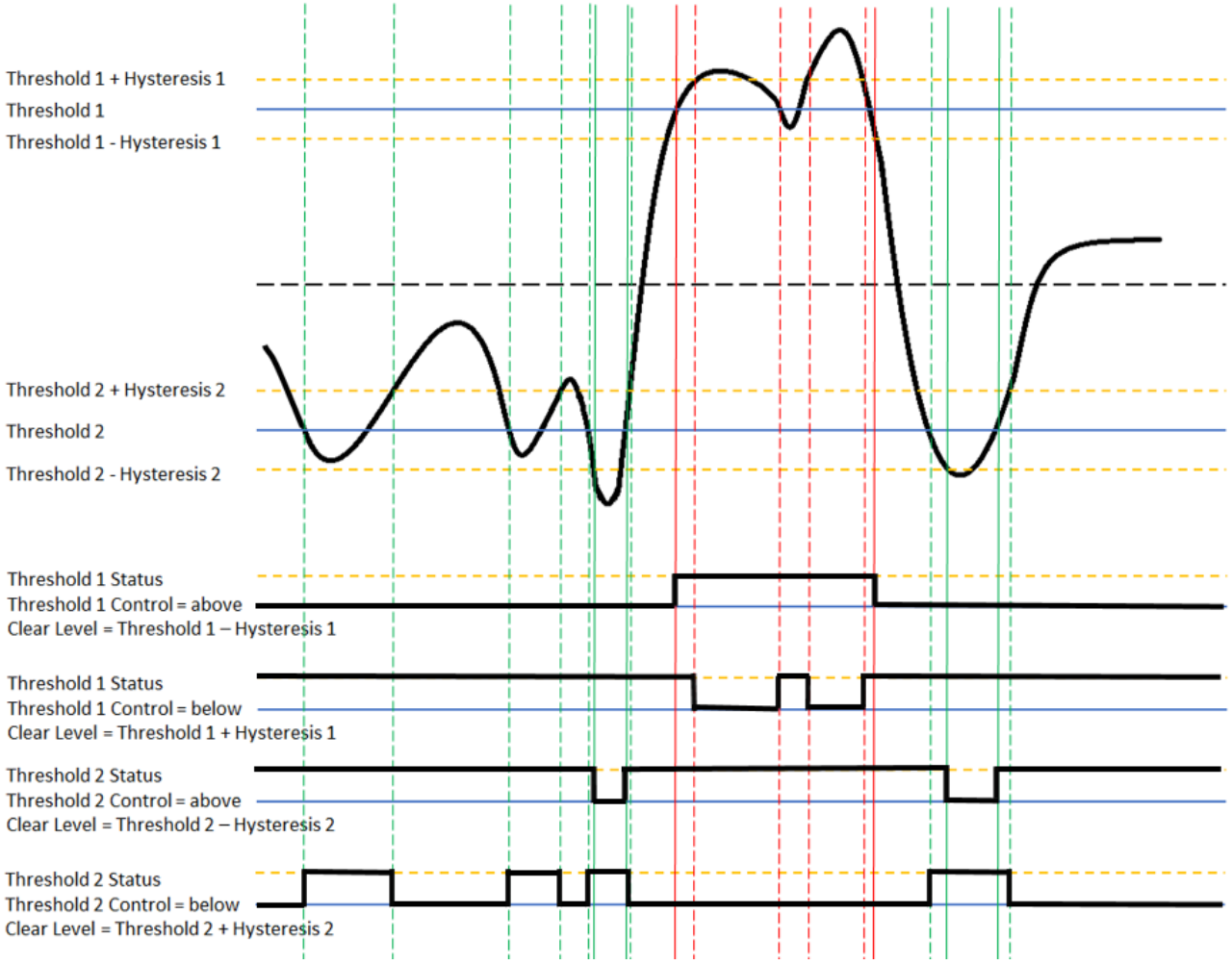


**Figure 1 - Threshold Programming with Hysteresis**

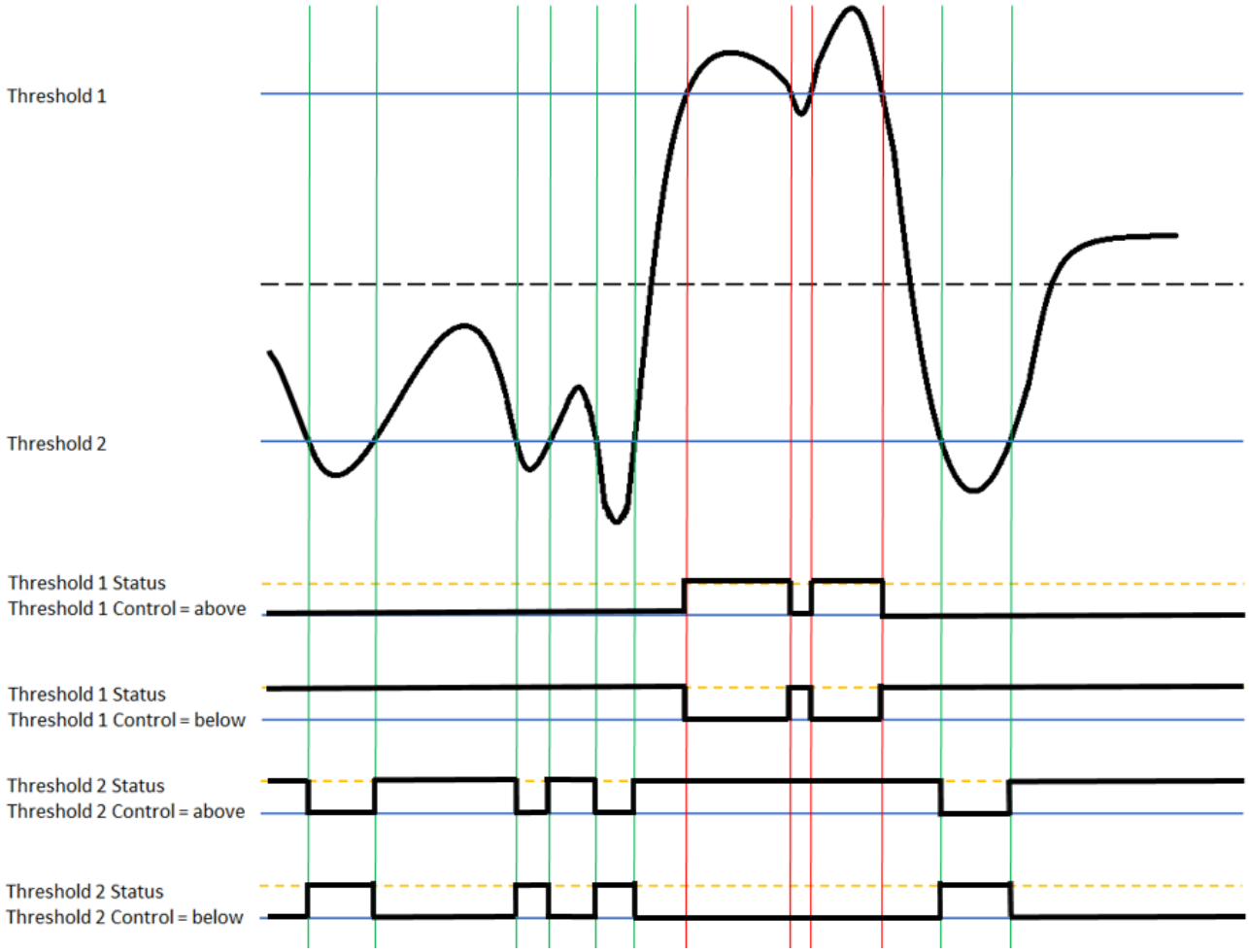


**Figure 2 - Threshold Programming with No Hysteresis**

## 2.2 Saturation Programming

A low and high saturation setting that can be independently programmed on the A/D modules. These saturation values are used to monitor the acquired data and set a status when the specified saturation is reached as well as setting the *A/D reading* to the saturation value. Saturation programming can be used to prevent the *A/D reading* from exceeding the saturation value. Refer to Figure 3 for illustrations of Saturation Programming.

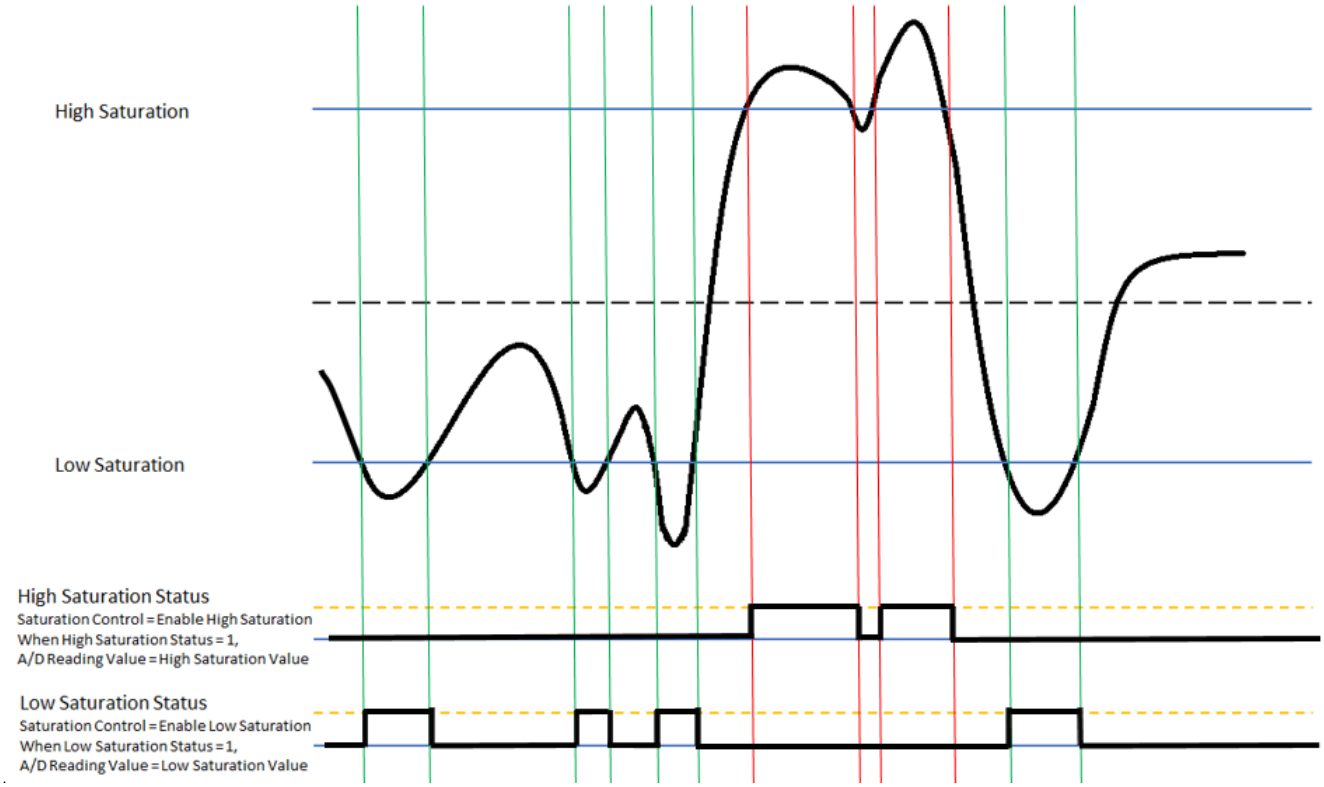


**Figure 3 - Saturation Programming**

# 3 Register Descriptions

The register descriptions provide the register name, Type, Data Range, Read or Write information, Initialized Value, and a description of the function.

## 3.1 Threshold Detect Programming Registers

There are two threshold and hysteresis registers that can be independently programmed on the A/D modules.

### *3.1.1 Threshold Detect Level*

The *Threshold Detect Level* registers sets the first and second threshold level values.

#### *3.1.1.1 Threshold Detect Level 1*

**Function:** Sets the first threshold level value.

**Type:** signed binary word (32-bit) (Integer Mode) or Single Precision Floating Point Value (IEEE-754) (Floating Point Mode)

**Data Range:** Voltage Threshold Level values are dependent on *Polarity and Range* settings for the channel.

***Enable Floating Point Mode:*** 0 (Integer Mode)

Unipolar: 0x0000 0000 to 0x0000 FFFF

Bipolar (2's compliment. 16-bit value sign extended to 32 bits): 0xFFFF 8000 to 0x0000 7FFF

***Enable Floating Point Mode:*** 1 (Floating Point Mode)

Single Precision Floating Point Value (IEEE-754)

**Read/Write:** R/W

**Initialized Value:** 90% of full scale (bipolar)

#### *3.1.1.2 Threshold Detect Level 2*

**Function:** Sets the second threshold level value.

**Type:** signed binary word (32-bit) (Integer Mode) or Single Precision Floating Point Value (IEEE-754) (Floating Point Mode)

**Data Range:** Voltage Threshold Level values are dependent on *Polarity and Range* settings for the channel.

***Enable Floating Point Mode:*** 0 (Integer Mode)

Unipolar: 0x0000 0000 to 0x0000 FFFF

Bipolar (2's compliment. 16-bit value sign extended to 32 bits): 0xFFFF 8000 to 0x0000 7FFF

***Enable Floating Point Mode:*** 1 (Floating Point Mode)

Single Precision Floating Point Value (IEEE-754)

**Read/Write:** R/W

**Initialized Value:** -90% of full scale (bipolar)

### 3.1.2 Threshold Detect Hysteresis

The Threshold Detect Hysteresis registers sets the first and second threshold hysteresis values. Note, the hysteresis value must be a positive value.

#### 3.1.2.1 Threshold Detect Hysteresis 1

**Function:** Sets the first threshold hysteresis value. This value must be positive.

**Type:** signed binary word (32-bit) or Single Precision Floating Point Value (IEEE-754) (Floating Point Mode)

**Data Range:** Voltage Threshold Hysteresis values are dependent on *Polarity and Range* settings for the channel.

***Enable Floating Point Mode:*** 0 (Integer Mode)

Unipolar: 0x0000 0000 to 0x0000 FFFF

Bipolar (2's compliment. 16-bit value sign extended to 32 bits): 0xFFFF 8000 to 0x0000 7FFF

***Enable Floating Point Mode:*** 1 (Floating Point Mode)

Single Precision Floating Point Value (IEEE-754)

**Read/Write:** R/W

**Initialized Value:** 0

#### 3.1.2.2 Threshold Detect Hysteresis 2

**Function:** Sets the second threshold hysteresis value. This value must be positive.

**Type:** signed binary word (32-bit) or Single Precision Floating Point Value (IEEE-754) (Floating Point Mode)

**Data Range:** Voltage Threshold Hysteresis values are dependent on *Polarity and Range* settings for the channel.

***Enable Floating Point Mode:*** 0 (Integer Mode)

Unipolar: 0x0000 0000 to 0x0000 FFFF

Bipolar (2's compliment. 16-bit value sign extended to 32 bits): 0xFFFF 8000 to 0x0000 7FFF

***Enable Floating Point Mode:*** 1 (Floating Point Mode)

Single Precision Floating Point Value (IEEE-754)

**Read/Write:** R/W

**Initialized Value:** 0

### 3.1.3 Threshold Detect Control

**Function:** Sets up detect control for the two thresholds for each channel.

**Type:** unsigned binary word (32-bit)

**Data Range:** 0x0000 0000 to 0xFFFF FFFF

**Read/Write:** R/W

**Initialized Value:** 0

**Operational Settings:** Set bit to **0** to detect **above** the threshold level. Set bit to **1** to detect **below** the threshold level.

| Threshold Detect Control | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **AD1-AD3** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| | | | | | | | | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** |
| | | | | | | | | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **AD4-AD6 and ADE-ADG** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| **Ch16** | | **Ch15** | | **Ch14** | | **Ch13** | | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **All A/D Modules** | | | | | | | | | | | | | | | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **Ch8** | | **Ch7** | | **Ch6** | | **Ch5** | | **Ch4** | | **Ch3** | | **Ch2** | | **Ch1** | |
| **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |

## 3.2 Saturation Programming Registers

A low and high saturation setting that can be independently programmed on the A/D modules.

### *3.2.1 Saturation Value*

The *Low Saturation Value* registers sets value to report as *A/D reading* and sets the Saturation Status bit when the A/D data is below the *low saturation value*. The *High Saturation Value* registers sets value to report as *A/D reading* and sets the Saturation Status bit when the A/D data is above the *high saturation value*.

#### *3.2.1.1 Low Saturation*

**Function:** Sets the *low saturation value*.

**Type:** signed binary word (32-bit) or Single Precision Floating Point Value (IEEE-754) (Floating Point Mode)

**Data Range:** Saturation Voltage values are dependent on *Polarity and Range* settings for the channel.

***Enable Floating Point Mode:*** 0 (Integer Mode)

Unipolar: 0x0000 0000 to 0x0000 FFFF

Bipolar (2's compliment. 16-bit value sign extended to 32 bits): 0xFFFF 8000 to 0x0000 7FFF

***Enable Floating Point Mode:*** 1 (Floating Point Mode)

Single Precision Floating Point Value (IEEE-754)

**Read/Write:** R/W

**Initialized Value:** 0

#### *3.2.1.2 High Saturation*

**Function:** Sets the *high saturation value*.

**Type:** signed binary word (32-bit) or Single Precision Floating Point Value (IEEE-754) (Floating Point Mode)

**Data Range:** Saturation Voltage values are dependent on *Polarity and Range* settings for the channel.

***Enable Floating Point Mode:*** 0 (Integer Mode)

Unipolar: 0x0000 0000 to 0x0000 FFFF

Bipolar (2's compliment. 16-bit value sign extended to 32 bits): 0xFFFF 8000 to 0x0000 7FFF

***Enable Floating Point Mode:*** 1 (Floating Point Mode)

Single Precision Floating Point Value (IEEE-754)

**Read/Write:** R/W

**Initialized Value:** 0

### 3.2.2 Saturation Control

**Function:** Sets up *saturation control* for the two saturation levels for each channel.

**Type:** unsigned binary word (32-bit)

**Data Range:** 0x0000 0000 to 0xFFFF FFFF

**Read/Write:** R/W

**Initialized Value:** 0

**Operational Settings:** Set bits to **1** to enable Saturation Control. Set bits to **0** to disable Saturation Control. Each channel control consists of two bits: *Low Saturation Control* ('Even' bits (B0, B2, B4,…)) and *High Saturation Control* ('Odd' bits (B1, B3, B5,…)).

| Saturation Control | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **AD1-AD3** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| | | | | | | | | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** |
| | | | | | | | | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **AD4-AD6 and ADE-ADG** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| **Ch16** | | **Ch15** | | **Ch14** | | **Ch13** | | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **All A/D Modules** | | | | | | | | | | | | | | | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **Ch8** | | **Ch7** | | **Ch6** | | **Ch5** | | **Ch4** | | **Ch3** | | **Ch2** | | **Ch1** | |
| **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |

## 3.3 Status and Interrupt

The A/D Module provides status registers for Threshold Detect and Saturation.

### *3.3.1 Threshold Detect Status*

There are four registers associated with the *Threshold Detect* Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt*.

**0** = Normal; **1** = Outside of threshold range. The status is created based on the values set in the *Threshold Detect 1* and *Threshold Detect 2* registers. Bits **D0** and **D1** represent if channel 1 is outside the threshold for *Threshold Detect 1* and *Threshold Detect 2* respectively, Bits **D2** and **D3** represent if channel 2 is outside the threshold for *Threshold Detect 1* and *Threshold Detect 2* respectively, etc. This pattern continues for all channels.

| **Threshold Detect Dynamic Status** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Threshold Detect Latched Status** | | | | | | | | | | | | | | | |
| **Threshold Detect Interrupt Enable** | | | | | | | | | | | | | | | |
| **Threshold Detect Set Edge/Level Interrupt** | | | | | | | | | | | | | | | |
| **AD1-AD3** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| | | | | | | | | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** |
| | | | | | | | | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **AD4-AD6 and ADE-ADG** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| **Ch16** | | **Ch15** | | **Ch14** | | **Ch13** | | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **All A/D Modules** | | | | | | | | | | | | | | | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **Ch8** | | **Ch7** | | **Ch6** | | **Ch5** | | **Ch4** | | **Ch3** | | **Ch2** | | **Ch1** | |
| **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** | **T2** | **T1** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |

**Function:** Sets the corresponding bit associated with the channel's Threshold Detect error.
**Type:** unsigned binary word (32-bit)
**Data Range:** 0x0000 0000 to 0x00FF FFFF
**Read/Write:** R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)
**Initialized Value:** 0

### 3.3.2 Saturation Status

There are four registers associated with the Saturation Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt*.

**0** = Normal; **1** = Outside of saturation range. The status is created based on the values set in the *Low Saturation* and *High Saturation* registers. Bits **D0** and **D1** represent if channel 1 is outside the voltage for *Low Saturation* and *High Saturation* respectively, Bits **D2** and **D3** represent if channel 2 is outside the voltage for *Low Saturation* and *High Saturation* respectively, etc. This pattern continues for all channels.

| **Saturation Dynamic Status** | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Saturation Latched Status** | | | | | | | | | | | | | | | |
| **Saturation Interrupt Enable** | | | | | | | | | | | | | | | |
| **Saturation Set Edge/Level Interrupt** | | | | | | | | | | | | | | | |
| **AD1-AD3** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| | | | | | | | | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** |
| | | | | | | | | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **AD4-AD6 and ADE-ADG** | | | | | | | | | | | | | | | |
| **D31** | **D30** | **D29** | **D28** | **D27** | **D26** | **D25** | **D24** | **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** |
| **Ch16** | | **Ch15** | | **Ch14** | | **Ch13** | | **Ch12** | | **Ch11** | | **Ch10** | | **Ch9** | |
| **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |
| **All A/D Modules** | | | | | | | | | | | | | | | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **Ch8** | | **Ch7** | | **Ch6** | | **Ch5** | | **Ch4** | | **Ch3** | | **Ch2** | | **Ch1** | |
| **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** | **High** | **Low** |
| **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **D** |

**Function:** Sets the corresponding bit associated with the channel's Saturation error.
**Type:** unsigned binary word (32-bit)
**Data Range:** 0x0000 0000 to 0x00FF FFFF
**Read/Write:** R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)
**Initialized Value:** 0

# 4 Function Register Map

Key: ***Bold Italic = Configuration/Control***

**Bold Underline = Status**

*When an event is detected, the bit associated with the event is set in this register and will remain set until the user clears the event bit. Clearing the bit requires writing a 1 back to the specific bit that was set when read (i.e. write-1-to-clear, writing a '1' to a bit set to '1' will set the bit to '0').

## 4.1 Threshold Detect Programming Registers

| All A/D Modules | | | | | |
|---|---|---|---|---|---|
| 0x1980 | ***Threshold Detect Level 1 Ch 1**** | R/W | 0x1A00 | ***Threshold Detect Level 1 Hysteresis Ch 1**** | R/W |
| 0x1984 | ***Threshold Detect Level 1 Ch 2**** | R/W | 0x1A04 | ***Threshold Detect Level 1 Hysteresis Ch 2**** | R/W |
| 0x1988 | ***Threshold Detect Level 1 Ch 3**** | R/W | 0x1A08 | ***Threshold Detect Level 1 Hysteresis Ch 3**** | R/W |
| 0x198C | ***Threshold Detect Level 1 Ch 4**** | R/W | 0x1A0C | ***Threshold Detect Level 1 Hysteresis Ch 4**** | R/W |
| 0x1990 | ***Threshold Detect Level 1 Ch 5**** | R/W | 0x1A10 | ***Threshold Detect Level 1 Hysteresis Ch 5**** | R/W |
| 0x1994 | ***Threshold Detect Level 1 Ch 6**** | R/W | 0x1A14 | ***Threshold Detect Level 1 Hysteresis Ch 6**** | R/W |
| 0x1998 | ***Threshold Detect Level 1 Ch 7**** | R/W | 0x1A18 | ***Threshold Detect Level 1 Hysteresis Ch 7**** | R/W |
| 0x199C | ***Threshold Detect Level 1 Ch 8**** | R/W | 0x1A1C | ***Threshold Detect Level 1 Hysteresis Ch 8**** | R/W |
| 0x19A0 | ***Threshold Detect Level 1 Ch 9**** | R/W | 0x1A20 | ***Threshold Detect Level 1 Hysteresis Ch 9**** | R/W |
| 0x19A4 | ***Threshold Detect Level 1 Ch 10**** | R/W | 0x1A24 | ***Threshold Detect Level 1 Hysteresis Ch 10**** | R/W |
| 0x19A8 | ***Threshold Detect Level 1 Ch 11**** | R/W | 0x1A28 | ***Threshold Detect Level 1 Hysteresis Ch 11**** | R/W |
| 0x19AC | ***Threshold Detect Level 1 Ch 12**** | R/W | 0x1A2C | ***Threshold Detect Level 1 Hysteresis Ch 12**** | R/W |
| **AD4-AD4, ADE-ADG** | | | | | |
| 0x19B0 | ***Threshold Detect Level 1 Ch 13**** | R/W | 0x1A30 | ***Threshold Detect Level 1 Hysteresis Ch 13**** | R/W |
| 0x19B4 | ***Threshold Detect Level 1 Ch 14**** | R/W | 0x1A34 | ***Threshold Detect Level 1 Hysteresis Ch 14**** | R/W |
| 0x19B8 | ***Threshold Detect Level 1 Ch 15**** | R/W | 0x1A38 | ***Threshold Detect Level 1 Hysteresis Ch 15**** | R/W |
| 0x19BC | ***Threshold Detect Level 1 Ch 16**** | R/W | 0x1A3C | ***Threshold Detect Level 1 Hysteresis Ch 16**** | R/W |

| All A/D Modules | | | | | |
|---|---|---|---|---|---|
| 0x1A80 | ***Threshold Detect Level 2 Ch 1**** | R/W | 0x1B00 | ***Threshold Detect Level 2 Hysteresis Ch 1**** | R/W |
| 0x1A84 | ***Threshold Detect Level 2 Ch 2**** | R/W | 0x1B04 | ***Threshold Detect Level 2 Hysteresis Ch 2**** | R/W |
| 0x1A88 | ***Threshold Detect Level 2 Ch 3**** | R/W | 0x1B08 | ***Threshold Detect Level 2 Hysteresis Ch 3**** | R/W |
| 0x1A8C | ***Threshold Detect Level 2 Ch 4**** | R/W | 0x1B0C | ***Threshold Detect Level 2 Hysteresis Ch 4**** | R/W |
| 0x1A90 | ***Threshold Detect Level 2 Ch 5**** | R/W | 0x1B10 | ***Threshold Detect Level 2 Hysteresis Ch 5**** | R/W |
| 0x1A94 | ***Threshold Detect Level 2 Ch 6**** | R/W | 0x1B14 | ***Threshold Detect Level 2 Hysteresis Ch 6**** | R/W |
| 0x1A98 | ***Threshold Detect Level 2 Ch 7**** | R/W | 0x1B18 | ***Threshold Detect Level 2 Hysteresis Ch 7**** | R/W |
| 0x1A9C | ***Threshold Detect Level 2 Ch 8**** | R/W | 0x1B1C | ***Threshold Detect Level 2 Hysteresis Ch 8**** | R/W |
| 0x1AA0 | ***Threshold Detect Level 2 Ch 9**** | R/W | 0x1B20 | ***Threshold Detect Level 2 Hysteresis Ch 9**** | R/W |
| 0x1AA4 | ***Threshold Detect Level 2 Ch 10**** | R/W | 0x1B24 | ***Threshold Detect Level 2 Hysteresis Ch 10**** | R/W |
| 0x1AA8 | ***Threshold Detect Level 2 Ch 11**** | R/W | 0x1B28 | ***Threshold Detect Level 2 Hysteresis Ch 11**** | R/W |
| 0x1AAC | ***Threshold Detect Level 2 Ch 12**** | R/W | 0x1B2C | ***Threshold Detect Level 2 Hysteresis Ch 12**** | R/W |
| **AD4-AD4, ADE-ADG** | | | | | |
| 0x1AB0 | ***Threshold Detect Level 2 Ch 13**** | R/W | 0x1B30 | ***Threshold Detect Level 2 Hysteresis Ch 13**** | R/W |
| 0x1AB4 | ***Threshold Detect Level 2 Ch 14**** | R/W | 0x1B34 | ***Threshold Detect Level 2 Hysteresis Ch 14**** | R/W |
| 0x1AB8 | ***Threshold Detect Level 2 Ch 15**** | R/W | 0x1B38 | ***Threshold Detect Level 2 Hysteresis Ch 15**** | R/W |
| 0x1ABC | ***Threshold Detect Level 2 Ch 16**** | R/W | 0x1B3C | ***Threshold Detect Level 2 Hysteresis Ch 16**** | R/W |

| | | |
|---|---|---|
| 0x1C80 | *Threshold Detect Control* | R/W |

## 4.2 Saturation Programming Registers

| All A/D Modules | | | | | |
|---|---|---|---|---|---|
| 0x1B80 | *Low Saturation Value Ch 1*** | R/W | 0x1C00 | *High Saturation Value Ch 1*** | R/W |
| 0x1B84 | *Low Saturation Value Ch 2*** | R/W | 0x1C04 | *High Saturation Value Ch 2*** | R/W |
| 0x1B88 | *Low Saturation Value Ch 3*** | R/W | 0x1C08 | *High Saturation Value Ch 3*** | R/W |
| 0x1B8C | *Low Saturation Value Ch 4*** | R/W | 0x1C0C | *High Saturation Value Ch 4*** | R/W |
| 0x1B90 | *Low Saturation Value Ch 5*** | R/W | 0x1C10 | *High Saturation Value Ch 5*** | R/W |
| 0x1B94 | *Low Saturation Value Ch 6*** | R/W | 0x1C14 | *High Saturation Value Ch 6*** | R/W |
| 0x1B98 | *Low Saturation Value Ch 7*** | R/W | 0x1C18 | *High Saturation Value Ch 7*** | R/W |
| 0x1B9C | *Low Saturation Value Ch 8*** | R/W | 0x1C1C | *High Saturation Value Ch 8*** | R/W |
| 0x1BA0 | *Low Saturation Value Ch 9*** | R/W | 0x1C20 | *High Saturation Value Ch 9*** | R/W |
| 0x1BA4 | *Low Saturation Value Ch 10*** | R/W | 0x1C24 | *High Saturation Value Ch 10*** | R/W |
| 0x1BA8 | *Low Saturation Value Ch 11*** | R/W | 0x1C28 | *High Saturation Value Ch 11*** | R/W |
| 0x1BAC | *Low Saturation Value Ch 12*** | R/W | 0x1C2C | *High Saturation Value Ch 12*** | R/W |
| **AD4-AD4, ADE-ADG** | | | | | |
| 0x1BB0 | *Low Saturation Value Ch 13*** | R/W | 0x1C30 | *High Saturation Value Ch 13*** | R/W |
| 0x1BB4 | *Low Saturation Value Ch 14*** | R/W | 0x1C34 | *High Saturation Value Ch 14*** | R/W |
| 0x1BB8 | *Low Saturation Value Ch 15*** | R/W | 0x1C38 | *High Saturation Value Ch 15*** | R/W |
| 0x1BBC | *Low Saturation Value Ch 16*** | R/W | 0x1C3C | *High Saturation Value Ch 16*** | R/W |

| | | |
|---|---|---|
| 0x1C90 | *Saturation Control* | R/W |

## 4.3 Status Registers

**Threshold**

| | | |
|---|---|---|
| 0x0940 | Dynamic Status | R |
| 0x0944 | Latched Status* | R/W |
| 0x0948 | *Interrupt Enable* | R/W |
| 0x094C | *Set Edge/Level Interrupt* | R/W |

**Saturation**

| | | |
|---|---|---|
| 0x0960 | Dynamic Status | R |
| 0x0964 | Latched Status* | R/W |
| 0x0968 | *Interrupt Enable* | R/W |
| 0x096C | *Set Edge/Level Interrupt* | R/W |

## 4.4 Interrupt Register

The Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Memory Space and these addresses are absolute based on the module slot position. In other words, do not apply the Module Address offset to these addresses.

| | | | | | |
|---|---|---|---|---|---|
| 0x0550 | ***Module 1 Interrupt Vector 21 - Threshold*** | R/W | 0x0650 | ***Module 1 Interrupt Steering 21 - Threshold*** | R/W |
| 0x0558 | ***Module 1 Interrupt Vector 23 - Saturation*** | R/W | 0x0658 | ***Module 1 Interrupt Steering 23 - Saturation*** | R/W |
| 0x0750 | ***Module 2 Interrupt Vector 21 - Threshold*** | R/W | 0x0850 | ***Module 2 Interrupt Steering 21 - Threshold*** | R/W |
| 0x0758 | ***Module 2 Interrupt Vector 23 - Saturation*** | R/W | 0x0858 | ***Module 2 Interrupt Steering 23 - Saturation*** | R/W |
| 0x0950 | ***Module 3 Interrupt Vector 21 - Threshold*** | R/W | 0x0A50 | ***Module 3 Interrupt Steering 21 - Threshold*** | R/W |
| 0x0958 | ***Module 3 Interrupt Vector 23 - Saturation*** | R/W | 0x0A58 | ***Module 3 Interrupt Steering 23 - Saturation*** | R/W |
| 0x0B50 | ***Module 4 Interrupt Vector 21 - Threshold*** | R/W | 0x0C50 | ***Module 4 Interrupt Steering 21 - Threshold*** | R/W |
| 0x0B58 | ***Module 4 Interrupt Vector 23 - Saturation*** | R/W | 0x0C58 | ***Module 4 Interrupt Steering 23 - Saturation*** | R/W |
| 0x0D50 | ***Module 5 Interrupt Vector 21 - Threshold*** | R/W | 0x0D50 | ***Module 5 Interrupt Steering 21 - Threshold*** | R/W |
| 0x0D58 | ***Module 5 Interrupt Vector 23 - Saturation*** | R/W | 0x0D58 | ***Module 5 Interrupt Steering 23 - Saturation*** | R/W |
| 0x0F50 | ***Module 6 Interrupt Vector 21 - Threshold*** | R/W | 0x1050 | ***Module 6 Interrupt Steering 21 - Threshold*** | R/W |
| 0x0F58 | ***Module 6 Interrupt Vector 23 - Saturation*** | R/W | 0x1058 | ***Module 6 Interrupt Steering 23 - Saturation*** | R/W |

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# Status and Interrupts

# MODULE MANUAL

# Revision History

| Revision | Revision Date | Description | Author |
|---|---|---|---|
| A | 6/17/2019 | Initial release | GC |
| A1 | 4/22/2020 | ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates. | MC |

# Table of Contents

# 1 Status and Interrupts

Status registers indicate the detection of faults or events. The status registers can be channel bit-mapped or event bit-mapped. An example of a channel bit-mapped register is the BIT status register, and an example of an event bit-mapped register is the FIFO status register.

For those status registers that allow interrupts to be generated upon the detection of the fault or the event, there are four registers associated with each status: *Dynamic, Latched, Interrupt Enabled*, and *Set Edge/Level Interrupt*.

**Dynamic Status:** The *Dynamic Status* register indicates the *current* condition of the fault or the event. If the fault or the event is momentary, the contents in this register will be clear when the fault or the event goes away. The *Dynamic Status* register can be polled, however, if the fault or the event is sporadic, it is possible for the indication of the fault or the event to be missed.

**Latched Status:** The *Latched Status* register indicates whether the fault or the event *has occurred* and keeps the state until it is cleared by the user. Reading the *Latched Status* register is a better alternative to polling the *Dynamic Status* register because the contents of this register will not clear until the user commands to clear the specific bit(s) associated with the fault or the event in the *Latched Status* register. Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel/event) location will "clear" the bit (set the bit to **0**). When clearing the channel/event bits, it is strongly recommended to write back the same bit pattern as read from the *Latched Status* register. For example, if the channel bit-mapped *Latched Status* register contains the value 0x0000 0005, which indicates fault/event detection on channel 1 and 3, write the value 0x0000 0005 to the *Latched Status* register to clear the fault/event status for channel 1 and 3. Writing a "1" to other channels that are not set (example 0x0000 000F) may result in incorrectly "clearing" incoming faults/events for those channels (example, channel 2 and 4).

**Interrupt Enable:** If interrupts are preferred upon the detection of a fault or an event, enable the specific channel/event interrupt in the *Interrupt Enable* register. The bits in *Interrupt Enable* register map to the same bits in the *Latched Status* register. When a fault or event occurs, an interrupt will be fired. Subsequent interrupts will not trigger until the application acknowledges the fired interrupt by clearing the associated channel/event bit in the *Latched Status* register. If the interruptible condition is still persistent after clearing the bit, this may retrigger the interrupt depending on the *Edge/Level* setting.

**Set Edge/Level Interrupt:** When interrupts are enabled, the condition on retriggering the interrupt after the Latch Register is "cleared" can be specified as "edge" triggered or "level" triggered. Note, the Edge/Level Trigger also affects how the Latched Register value is adjusted after it is "cleared" (see 1.1.1).

- *Edge triggered*: An interrupt will be retriggered when the Latched Status register change from low (0) to high (1) state. Uses for edge-triggered interrupts would include transition detections (Low-to-High transitions, High-to-Low transitions) or fault detections. After "clearing" an interrupt, another interrupt will not occur until the next transition or the re-occurrence of the fault again.
- *Level triggered*: An interrupt will be generated when the Latched Status register remains at the high (1) state. Level-triggered interrupts are used to indicate that something needs attention.

## 1.1 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed with a unique number/identifier defined by the user such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism. In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

## 1.2 Interrupt Trigger Types

In most applications, limiting the number of interrupts generated is preferred as interrupts are costly, thus choosing the correct Edge/Level interrupt trigger to use is important.

Example 1: Fault detection

This example illustrates interrupt considerations when detecting a fault like an “open” on a line. When an “open” is detected, the system will receive an interrupt. If the “open” on the line is persistent and the trigger is set to “edge”, upon “clearing” the interrupt, the system will not re-generate another interrupt. If, instead, the trigger is set to “level”, upon “clearing” the interrupt, the system will re-generate another interrupt. Thus, in this case, it will be better to set the trigger type to “edge”.

Example 2: Threshold detection

This example illustrates interrupt considerations when detecting an event like reaching or exceeding the “high watermark” threshold value. In a communication device, when the number of elements received in the FIFO reaches the high-watermark threshold, an interrupt will be generated. Normally, the application would read the count of the number of elements in the FIFO and read this number of elements from the FIFO. After reading the FIFO data, the application would “clear” the interrupt. If the trigger type is set to “edge”, another interrupt will be generated only if the number of elements in FIFO goes below the “high watermark” after the “clearing” the interrupt and then fills up to reach the “high watermark” threshold value. Since receiving communication data is inherently asynchronous, it is possible that data can continue to fill the FIFO as the application is pulling data off the FIFO. If, at the time the interrupt is “cleared”, the number of elements in the FIFO is at or above the “high watermark”, no interrupts will be generated. In this case, it will be better to set the trigger type to “level”, as the purpose here is to make sure that the FIFO is serviced when the number of elements exceeds the high watermark threshold value. Thus, upon “clearing” the interrupt, if the number of elements in the FIFO is at or above the “high watermark” threshold value, another interrupt will be generated indicating that the FIFO needs to be serviced.

## 1.3 Dynamic and Latched Status Registers Examples

The examples in this section illustrate the differences in behavior of the Dynamic Status and Latched Status registers as well as the differences in behavior of Edge/Level Trigger when the Latched Status register is cleared.

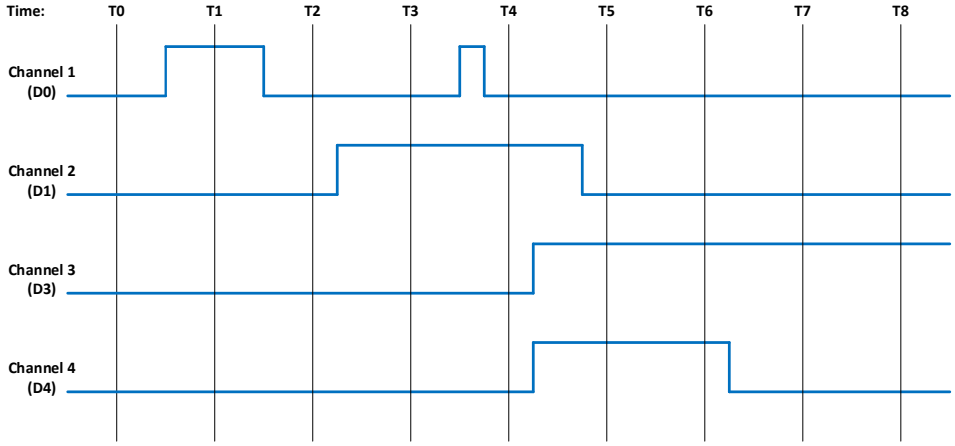


**Figure 1 - Example of Module's Channel-Mapped Dynamic and Latched Status States**

| Time | Dynamic Status | No Clearing of Latched Status | Clearing of Latched Status (Edge-Triggered) | | Clearing of Latched Status (Level-Triggered) | |
|---|---|---|---|---|---|---|
| | | Latched Status | Action | Latched Status | Action | Latched |
| **T0** | 0x0 | 0x0 | Read Latched Register | 0x0 | Read Latched Register | 0x0 |
| **T1** | 0x1 | 0x1 | Read Latched Register | 0x1 | | 0x1 |
| | | | Write 0x1 to Latched Register | | Write 0x1 to Latched Register | |
| | | | | *0x0* | | *0x1* |
| **T2** | 0x0 | 0x1 | Read Latched Register | 0x0 | Read Latched Register | 0x1 |
| | | | | | Write 0x1 to Latched Register | |
| | | | | | | *0x0* |
| **T3** | 0x2 | 0x3 | Read Latched Register | 0x2 | Read Latched Register | 0x2 |
| | | | Write 0x2 to Latched Register | | Write 0x2 to Latched Register | |
| | | | | *0x0* | | *0x2* |
| **T4** | 0x2 | 0x3 | Read Latched Register | 0x1 | Read Latched Register | 0x3 |
| | | | Write 0x1 to Latched Register | | Write 0x3 to Latched Register | |
| | | | | *0x0* | | *0x2* |
| **T5** | 0xC | 0xF | Read Latched Register | 0xC | Read Latched Register | 0xE |
| | | | Write 0xC to Latched Register | | Write 0xE to Latched Register | |
| | | | | *0x0* | | *0xC* |
| **T6** | 0xC | 0xF | Read Latched Register | 0x0 | Read Latched Register | 0xC |
| | | | | | Write 0xC to Latched Register | |
| | | | | | | *0xC* |
| **T7** | 0x4 | 0xF | Read Latched Register | 0x0 | Read Latched Register | 0xC |
| | | | | | Write 0xC to Latched Register | |
| | | | | | | *0x4* |
| **T8** | 0x4 | 0xF | Read Latched Register | 0x0 | Read Latched Register | 0x4 |

## 1.4 Interrupt Examples

The examples in this section illustrate the interrupt behavior with Edge/Level Trigger.

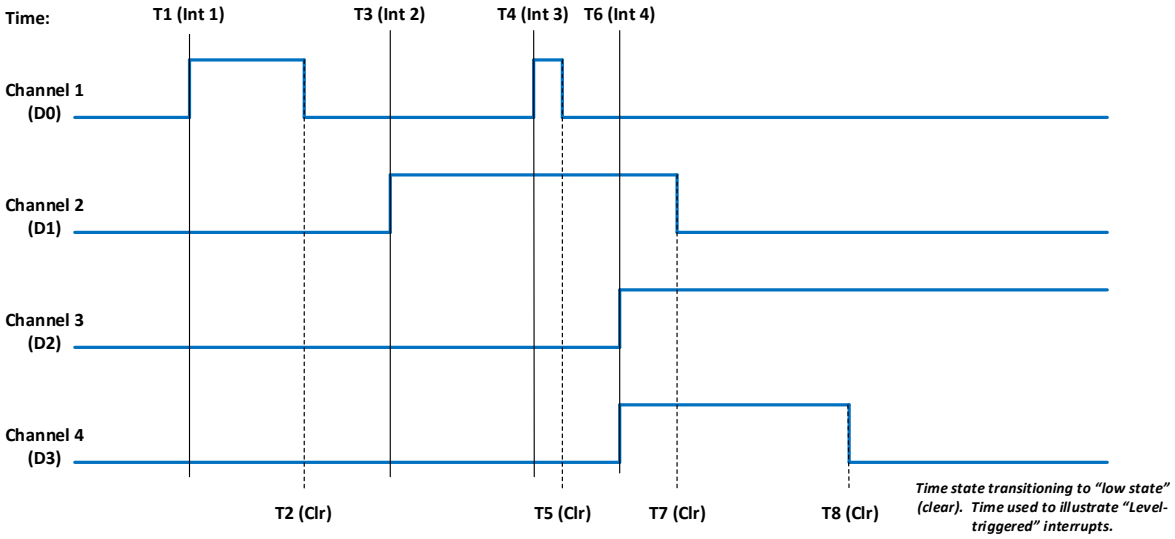


**Figure 2 - Illustration of Latched Status State for Module with 4-Channels with Interrupt Enabled**

| Time | Latched Status (Edge-Triggered – Clear Multi-Channel) Action | Latched | Latched Status (Edge-Triggered – Clear Single Channel) Action | Latched | Latched Status (Level-Triggered – Clear Multi-Channel) Action | Latched |
|---|---|---|---|---|---|---|
| **T1 (Int 1)** | **Interrupt Generated** Read Latched Registers | 0x1 | **Interrupt Generated** Read Latched Registers | 0x1 | **Interrupt Generated** Read Latched Registers | 0x1 |
| | Write 0x1 to Latched Register | | Write 0x1 to Latched Register | | Write 0x1 to Latched Register | |
| | | *0x0* | | *0x0* | ***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T2. | *0x1* |
| **T3 (Int 2)** | **Interrupt Generated** Read Latched Registers | 0x2 | **Interrupt Generated** Read Latched Registers | 0x2 | **Interrupt Generated** Read Latched Registers | 0x2 |
| | Write 0x2 to Latched Register | | Write 0x2 to Latched Register | | Write 0x2 to Latched Register | |
| | | *0x0* | | *0x0* | ***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T7. | *0x2* |
| **T4 (Int 3)** | **Interrupt Generated** Read Latched Registers | 0x1 | **Interrupt Generated** Read Latched Registers | 0x1 | **Interrupt Generated** Read Latched Registers | 0x3 |
| | Write 0x1 to Latched Register | | Write 0x1 to Latched Register | | Write 0x3 to Latched Register | |
| | | *0x0* | | *0x0* | ***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0x3 is reported in Latched Register until T5. | *0x3* |
| | | | | | ***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T7. | *0x2* |

| | | | | | | |
|---|---|---|---|---|---|---|
| **T6 (Int 4)** | **Interrupt Generated** Read Latched Registers | 0xC | **Interrupt Generated** Read Latched Registers | 0xC | **Interrupt Generated** Read Latched Registers | 0xE |
| | Write 0xC to Latched Register | | Write 0x4 to Latched Register | | Write 0xE to Latched Register | |
| | | *0x0* | ***Interrupt re-triggers*** Write 0x8 to Latched Register | *0x8* | ***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xE is reported in Latched Register until T7. | *0xE* |
| | | | | *0x0* | ***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xC is reported in Latched Register until T8. | *0xC* |
| | | | | | ***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0x4 is reported in Latched Register always. | *0x4* |

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